LINEAR TECHNOLOGY

Safe Hot Swapping Using the LTC1421

by Robert Reay and James Herr

When a circuit board is inserted into a live backplane, the large bypass capacitors on the board can draw huge inrush currents from the backplane power bus as they charge. The inrush current, on the order of 10 to 100 amps, can destroy the board's bypass capacitors, metal traces or connector pins. The inrush current can also cause a glitch on the backplane power bus, which may force all of the other boards in the system to reset. At the same time, the system data bus can be disrupted when the board's data pins make or break contact.

The LTC1421 can turn on up to three board supply voltages at a programmable rate, allowing boards to be safely inserted in or removed from a live backplane. The chip also provides board connection sensing, a method for halting the system data bus during insertion or removal, flexible supply voltage monitoring, power-on reset outputs, short-circuit protection and digital input or push-button power cycling control.

Typical Application

Figure 1 shows a typical application using the LTC1421. The power supplies on the board are controlled by placing external N-channel pass transistors Q1, Q2 and Q3 in the power path for V_{CC}, V_{DD} and V_{EE}, where V_{CC} and V_{DD} can range from 3.0V to 12.0V. By ramping the gates of the pass transistors up or down at a controlled rate, the transient surge current ($I = C \times dv/dt$) drawn from the main backplane supply will be limited to a safe value.

The LTC1421 is designed for use with a staggered 3-level connector. Ground should make connection first to discharge any static buildup. V_{CC}, V_{DD}, V_{EE} and DISABLE should make connection second and the data bus and all other pins last. The connection sense pins $\overline{CON1}$ and $\overline{CON2}$ must be located on opposite ends of the connector because most people will rock the board back and forth during insertion.

The system timing is shown in Figure 2. When the supply pins make contact, (Figure 2, time point 1), the LTC1421 prevents transistors Q1 and Q2 from turning on by holding their gates (GATELO and GATEHI) at ground, while C3 and R4 keep Q3 off by pulling its gate to –12V. The Schottky diode in the output stage of CPON allows the pin to be pulled below ground. The two connection sense pins, $\overline{CON1}$ and $\overline{CON2}$, are initially pulled to V_{CCLO} by 10k pull-up resistors. PWRGD and $\overline{RESET}$ are held low while V_{CCLO} and V_{CCHI} are pulled to ground by internal transistors N1 and N2. At the same time, DISABLE is pulled high, turning on transistor Q4, which will halt traffic on the backplane data bus before the data pins make contact. $\overline{CON1}$ and $\overline{CON2}$ are the last pins to make contact and are shorted to ground on the backplane side of the connector. After

Issue Highlights

This issue of *Linear Technology* features more exciting new products from Linear Technology's design team. Our lead article explains "safe hot swapping" using the LTC1421 hot swap controller. This device prevents inrush currents that can destroy components and traces. It also eliminates glitches that disrupt the system bus when a circuit board is plugged into a "live" backplane. The LTC1421 can turn on up to three board supply voltages at programmable rates. The part provides board connection sensing, which can be used to halt the system bus during board insertion or removal, power-on reset outputs, short-circuit protection and digital input or push-button power cycling.

Also in this issue, we have an in-depth examination of the "Care and Feeding of High Performance ADCs," such as the 1.25Msps, 12-bit LTC1410. Designers will be finding many new applications for these parts because of their excellent specifications and attractive pricing. This article provides the layout, bypassing and other design techniques that will allow you to obtain maximum performance from these precision parts.

In the area of power products, we introduce the LTC1433 and LTC1434 high efficiency, constant-frequency monolithic buck converters. These devices achieve high efficiency and constant frequency at low load currents using the Adaptive Power™ mode first introduced in the LTC1435–LTC1439 family of DC/DC controllers.

Also new are a pair of interface products, the LTC1343 and LTC1344. The LTC1343 contains four drivers and four receivers and the LTC1344 contains six switchable resistive terminators. Together, these two devices can implement a software-selectable, multiple-protocol serial port that supports a wide range of protocols.

This month, we have a generous helping of Design Ideas, including two battery chargers, plus a constant-voltage load box for battery simulation; some unusual amplifier

LTC in the News...

"Technology stocks have fallen so far in recent months that they have become tantalizing to bottom-fishing value investors, who rarely get a chance to buy normally pricey computer and semiconductor makers," wrote E.S. Browning, staff reporter of the *Wall Street Journal*, in an article in the *Dow Jones Newswire*. "These companies now look like real bargains," he writes.

Chicago Corp. analyst David Wu said, "Linear is a good company in a great business with high barriers to entry." He added that he looks for a resumption of double-digit growth after a period of adjustment, which could take a year.

Even more bullish on Linear is Ed Jamieson, manager of the Franklin Small Cap Growth fund, who told *Barron's Financial Weekly* in July that he believes LTC can produce 25%–50% returns in the next 12 months. "Historically, its market grew 35% a year.... It's crazy not to think this company will reemerge."

The perceptions of these shrewd industry observers are turning out to be prophetic. On July 23, LTC announced that net sales for its fiscal year ended June 30 were a record $377,771,000, an increase of 43% over the previous year. The company also reported record net income for the year of $133,964,000 or $1.72 per share, an increase of 58% over $84,696,000 or $1.11 per share reported for fiscal 1995.

According to Robert H. Swanson, Jr., president and CEO of Linear Technology Corp., "1996 was a very strong year for us in sales, profits and cash growth. Our rate of sales growth was higher than our historical average in response to a very robust market early in the year. The current environment is balancing out some of this accelerated growth and our sales for the fourth quarter were less than the previous quarter for the first time in ten years," Swanson said.

"Net income as a percentage of sales continued to be the strongest in the industry. The long term prospects for our business are excellent and we continue to invest in the plant infrastructure and technical talent to maximize our opportunities. In the short term, however, reduced backlog and shorter lead times have caused the business to be more dependent on orders that are received and shipped in the same quarter," Swanson said. *LT*

applications featuring the LT1210 and the LT1336; a micropower voltage-to-frequency converter; a circuit for measuring small capacitance changes and several power supply designs.

Also new from Linear Technology this month are the LinearView™ CD-ROM and the Micropower SwitcherCAD™ design software.

The LinearView CD-ROM contains all product data from Linear Technology's Databooks (volumes I–IV) and applications information from Linear's Applications Handbooks (volumes I and II), plus the complete collections of Design Notes and back issues of *Linear Technology* magazine.

MicroPower SwitcherCAD is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components that surround the DC/DC converter.

See page 43 for ordering information for either LinearView or Micropower SwitcherCAD.

As always, we welcome your questions and comments. Call (408) 432-1900 to talk to the authors of any of this issue's articles about your application needs. *LT*

Hot Swapping, continued from page 1

they have stopped bouncing (Figure 2, time point 2), the LTC1421 will wait for 20ms.

At the end of 20ms, if V_{CCLO} and V_{CCHI} have exceeded the undervoltage lockout threshold (2.45V), and V_{OUTLO} is less than 100mV above ground, the LTC1421 is ready to turn on the supplies (Figure 2, time point 3). A 20µA reference current is connected to the RAMP pin, the charge pumps turn on, CPON pulls high and the voltage at GATEHI begins to rise with a slope equal to $20µA/C_{RAMP}$. The voltage at the GATELO pin is clamped one Schottky diode drop below GATEHI. The ramp time for each supply is $t = (V_{SUPPLY} \times C_{RAMP})/20µA$. Because the N-channel transistors Q1 and Q2 act as source followers, the voltage at V_{OUTLO} and V_{OUTHI} have the same ramp rate. Therefore, the inrush current into the bypass capacitors C4 and C5 is $I = (C_{BYPASS} \times 20µA)/C_{RAMP}$. The internal charge pumps are designed to provide at least 8V of gate drive to Q1 and Q2.

The negative supply voltage is controlled using the CPON pin. When the board first makes connection, transistor Q3 is turned off by R4 and C3. After the charge pump turns on, CPON is pulled to V_{CCLO} and the gate of Q3 ramp up with a time constant determined by R4, R5 and C3.
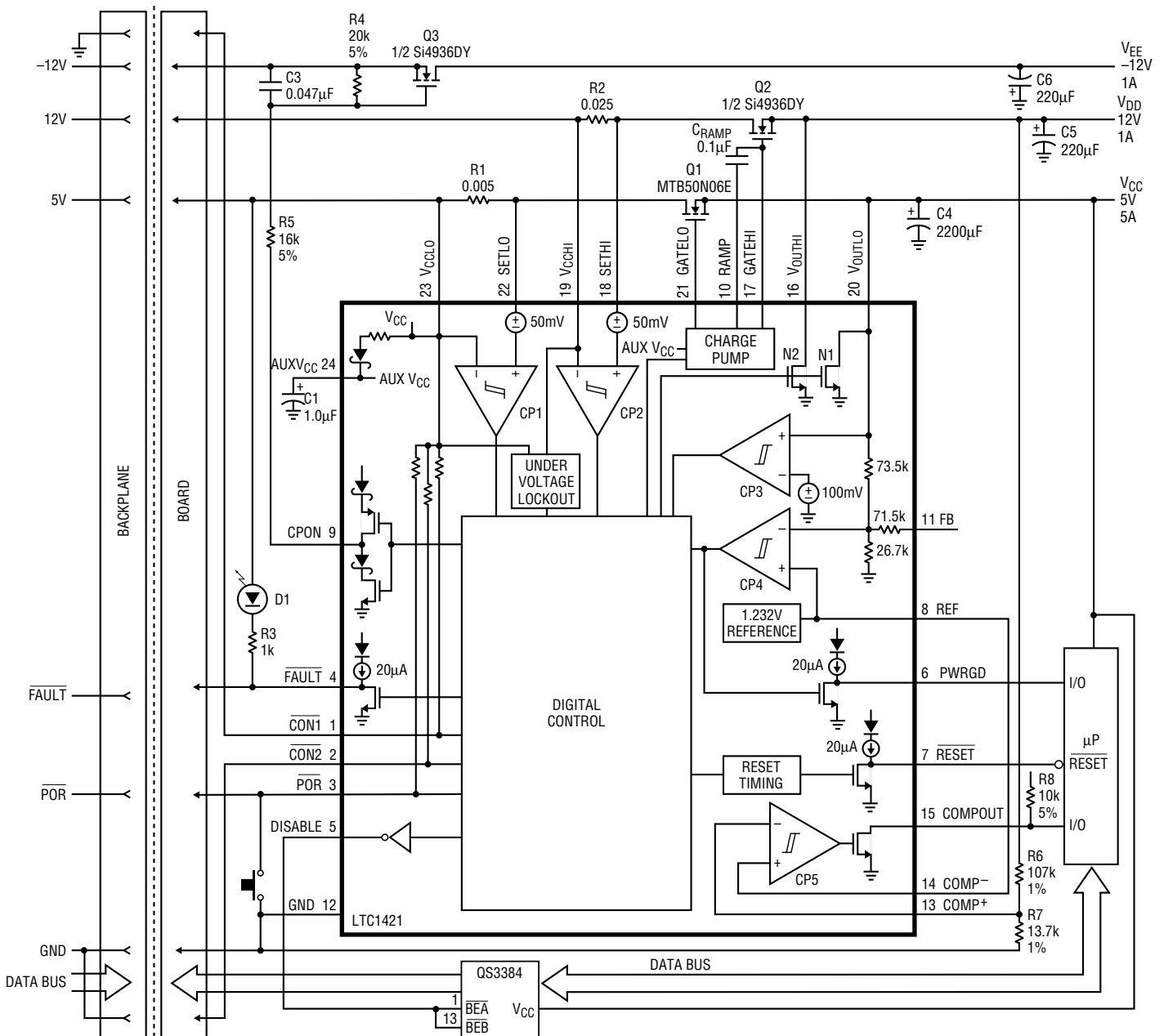

Figure 1. LTC1421 typical application

As soon as V_{CCLO} reaches the 4.65V reset threshold, (Figure 2, time point 4), the PWRGD signal immediately pulls high. After a 200ms delay, the $\overline{RESET}$ signal pulls high, (Figure 2, time point 6), and the DISABLE pin pulls low, thus enabling the system data bus. In this application, the free comparator, CP5, is used to monitor the 12V supply. When V_{OUTHI} reaches 10.8V, the COMPOUT signal pulls high (Figure 2, time point 5).

Monitoring
The Supply Voltages

The LTC1421 features a 1.232V reference, internal resistor divider from V_{CCLO} and precision voltage comparators CP4 and CP5 (Figure 1) to monitor the supply voltages. The reset thresh-

old voltage for V_{OUTLO} is determined by the FB pin connection as summarized in Table 1.

When the V_{OUTLO} voltage rises above its reset threshold voltage, the comparator (CP4) output goes low, and PWRGD is immediately pulled high to V_{CCLO} by a weak pull-up current source or external resistor. After a 200ms delay, $\overline{RESET}$ is pulled high.
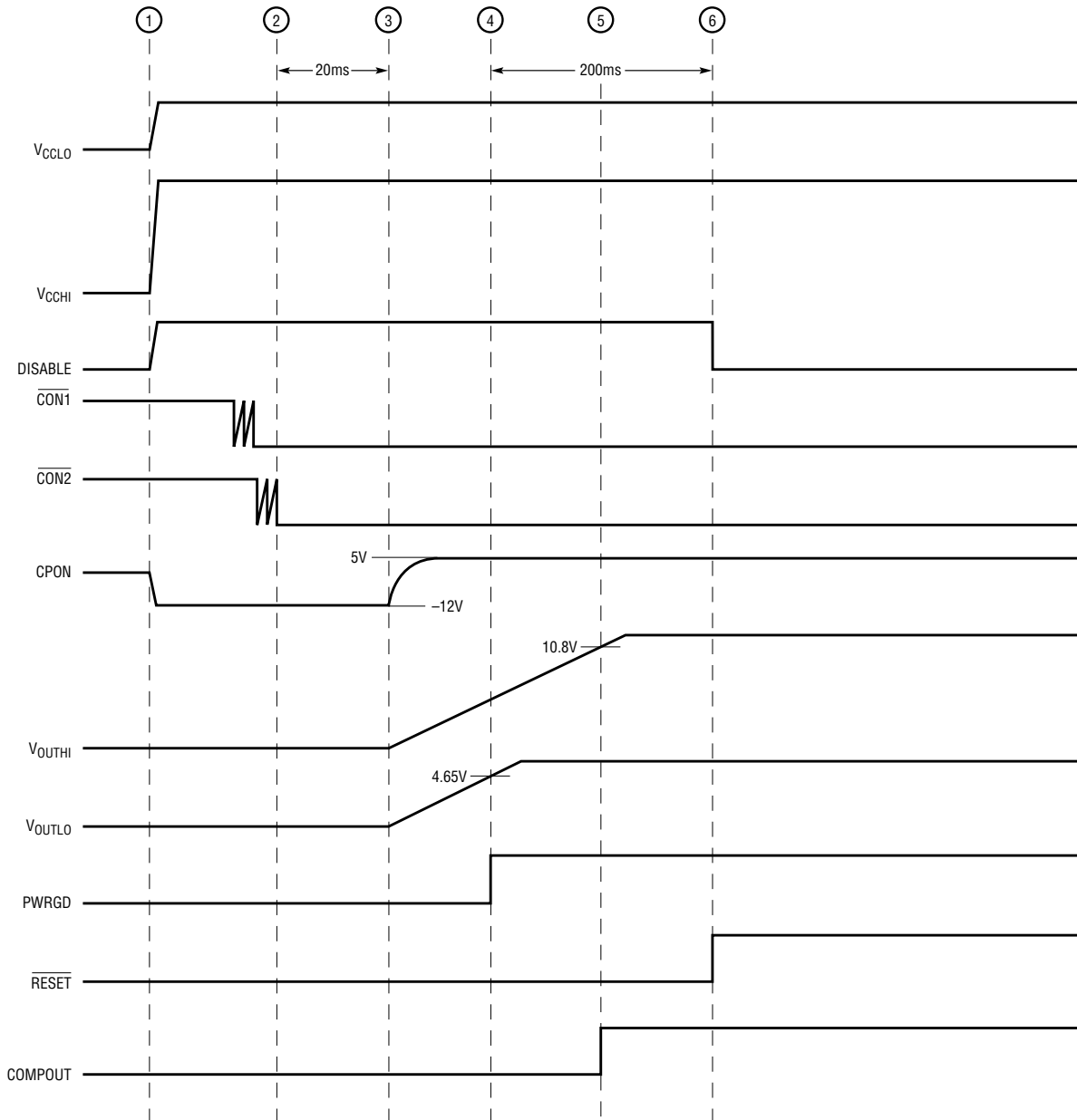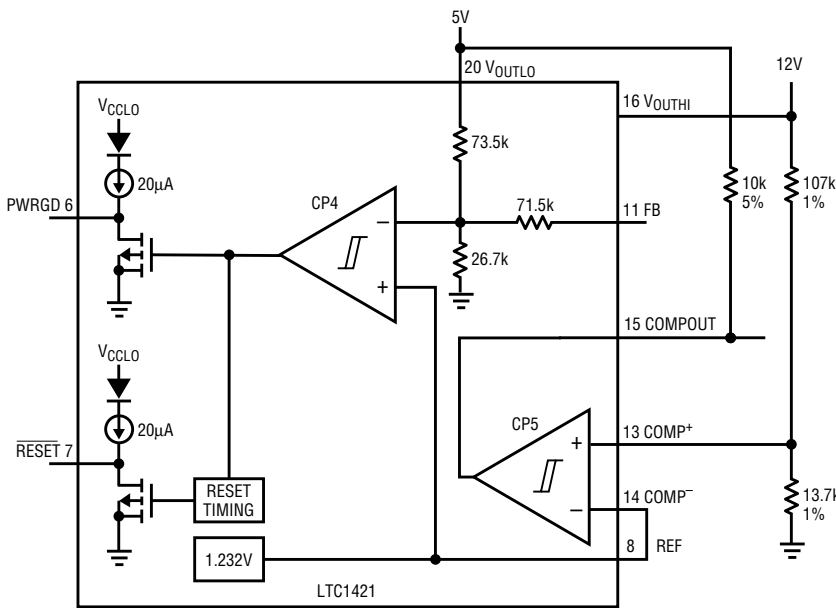

Figure 2. Typical insertion timing

Figure 3. Monitoring a 12V supply with a 10.8V threshold; the 5V supply generates a reset when it dips below 4.65V.

The weak pull-up current sources to V_{CCLO} on PWRGD and $\overline{RESET}$ have a series diode so the pins can be pulled above V_{CCLO} by an external pull-up resistor without forcing current back into V_{CCLO}.

When V_{CCLO} drops below its reset threshold, the comparator (CP4) output goes high, and PWRGD immediately pulls low. After a 64µs delay, $\overline{RESET}$ is pulled low. The $\overline{RESET}$ delay allows the PWRGD signal to be used as an early warning that a reset is about to occur. If the PWRGD signal is used as an interrupt input to a microprocessor, a short power-down routine can be run before the reset occurs.

The uncommitted voltage comparator (CP5) can be used to monitor output voltages other than V_{OUTLO}. Figure 3 shows how the comparator can be used to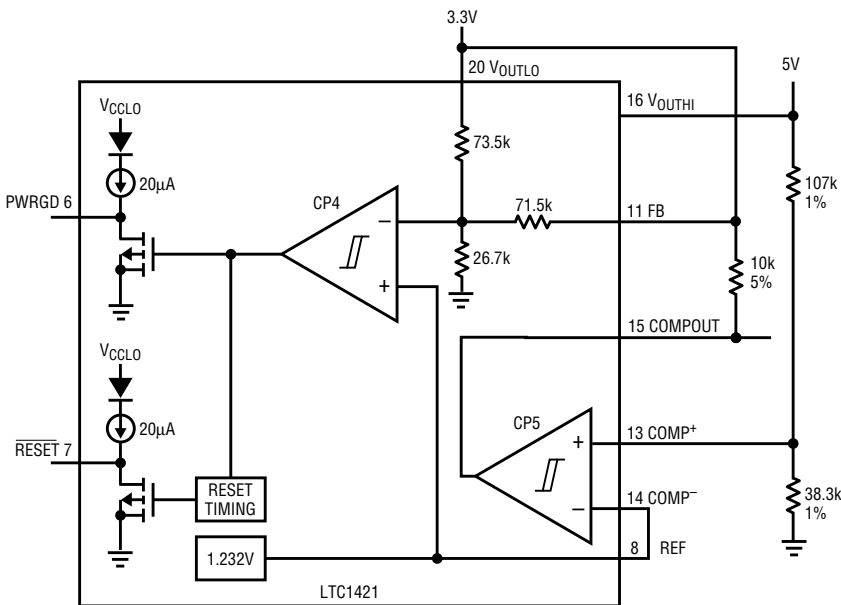 monitor a 12V supply with a 10.8V threshold, while the 5V supply generates a reset when it dips below 4.65V. The FB pin is left floating.

Figure 4 shows how to monitor a 5V supply with a 4.65V threshold, while the 3.3V supply generates a reset when it dips below 2.9V. The FB pin is tied to V_{CCLO}.

Figure 5 shows how the comparator can be used to generate a reset when the 12V supply drops below 10.8V. The 5V supply also generates a reset when it dips below 4.65V. When 12V dips below 10.8V, COMPOUT will pull the FB pin low, setting the internal threshold voltage for CP5 to 5.88V. Since V_{OUTLO} is less than 5.88V, PWRGD immediately goes low, followed by $\overline{RESET}$ 64µs later.

Figure 6 shows how comparator CP5 can be used to override the internal reset voltage threshold. A 5k resistor is tied from the FB pin to V_{OUTLO}, setting the internal threshold to about 2.9V. The new reset threshold voltage is set by the external resistor divider connected to CP5, in this case 4.5V. When V_{OUTLO} drops below the new threshold voltage, COMPOUT pulls FB to ground, changing the internal threshold to 5.88V and generating a reset.

Finally, Figure 7 shows how CP5 can be used to monitor a negative supply voltage.

Electronic Circuit Breaker

The LTC1421 features an electronic circuit-breaker function that protects against short circuits or excessive current on the supplies by placing sense resistors (R1 and R2) between the supply input and sense pin of either supply. The circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than 20µs. When the

Figure 4. Monitoring a 5V supply with a 4.65V threshold; the 3.3V supply generates a reset when it dips below 2.9V.

Table 1. Reset voltage thresholds

Feedback Pin	V_{OUTLO} Reset Voltage
Floating	4.65V
V_{OUTLO}	2.90V
GND	5.88V

circuit breaker trips, both N-channel transistors (Q1 and Q2) are immediately turned off and the $\overline{FAULT}$ pin is pulled low. When V_{CCLO} drops below the 4.65V threshold, PWRGD is pulled low and $\overline{RESET}$ is pulled low 64µs later. The chip will remain in the tripped state until a power-on reset is generated, (pulling the $\overline{POR}$ pin low momentarily), or the power on V_{CCHI} and V_{CCLO} is cycled. If the circuit breaker feature is not used, V_{CCLO} can be shorted to SETLO and V_{CCHI} to SETHI.

Auxiliary V_{CC}

When a short circuit occurs on the board, it is possible to draw enough current to cause the backplane supply voltage to collapse to a low enough voltage that the LTC1421 gate drive circuitry is unable to shut off the N-channel pass transistors (Q1 and Q2). This could also happen if V_{CCLO} breaks contact but V_{CCHI} remains connected.

To prevent the system from freezing up in a permanent short condition, the gate-discharge circuitry inside the LTC1421 is powered from the AUXV$_{CC}$ pin, which, in turn, is powered from V_{CCLO} through an internal Schottky diode and current limiting resistor (Figure 8).

When V_{CCLO} collapses, there is enough energy stored on the 1.0µF capacitor connected to AUXV$_{CC}$ to keep the gate discharge circuitry alive long enough to fully turn off the external N-channels.

Power-On Reset

The $\overline{POR}$ can be used to completely cycle the power supplies on the board or to reset the electronic circuit-breaker feature. The $\overline{POR}$ pin can be connected to a grounded push button or toggle switch, or to a logic signal from the backplane through the connector.
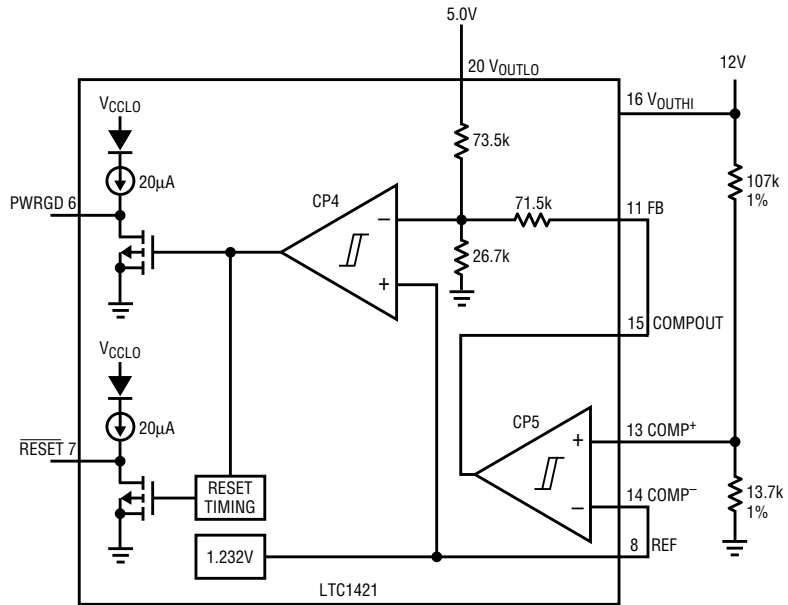
Figure 5. Generating a reset when the 12V supply drops below 10.8V; the 5V supply also generates a reset when it dips below 4.65V.

Figure 9 shows the typical power-on reset cycle. After the $\overline{POR}$ pin is held low for 20ms, internal transistors N1 and N2 are turned on to start discharging V_{OUTLO} and V_{OUTHI}. At the same time, GATEHI and GATELO are also actively pulled down internally, while CPON goes low. When V_{OUTHI} reaches the reset threshold, the COMPOUT pin pulls low (time point 3). When V_{OUTLO} reaches the reset threshold, PWRGD immediately pulls low, followed by $\overline{RESET}$ 64µs later. When V_{OUTLO} is discharged within 100mV of ground, the LTC1421 will reset and start a normal power-up sequence.
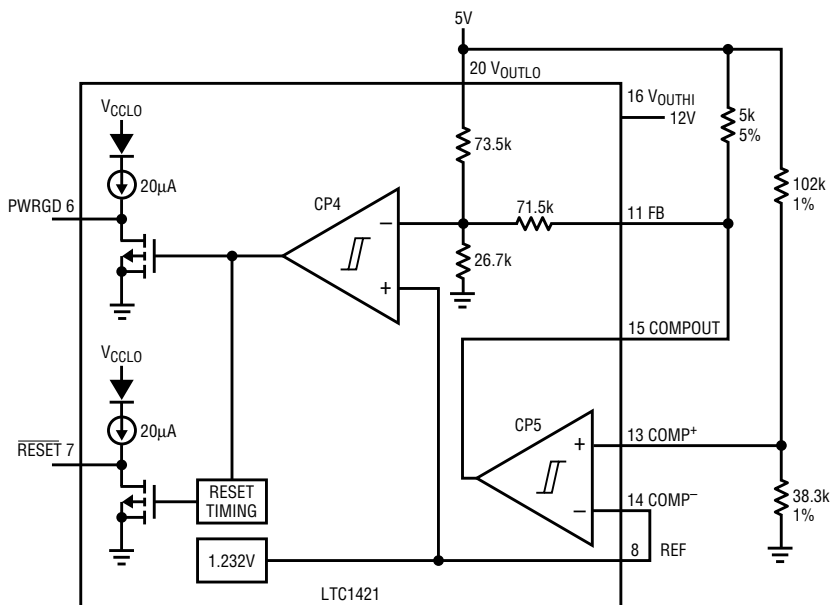
Figure 6. CP5 can be used to override the internal reset voltage threshold. A 5k resistor is tied from the FB pin to V_{OUTLO}, setting the internal threshold to about 2.9V. The new reset threshold voltage is set by the external resistor divider connected to CP5.
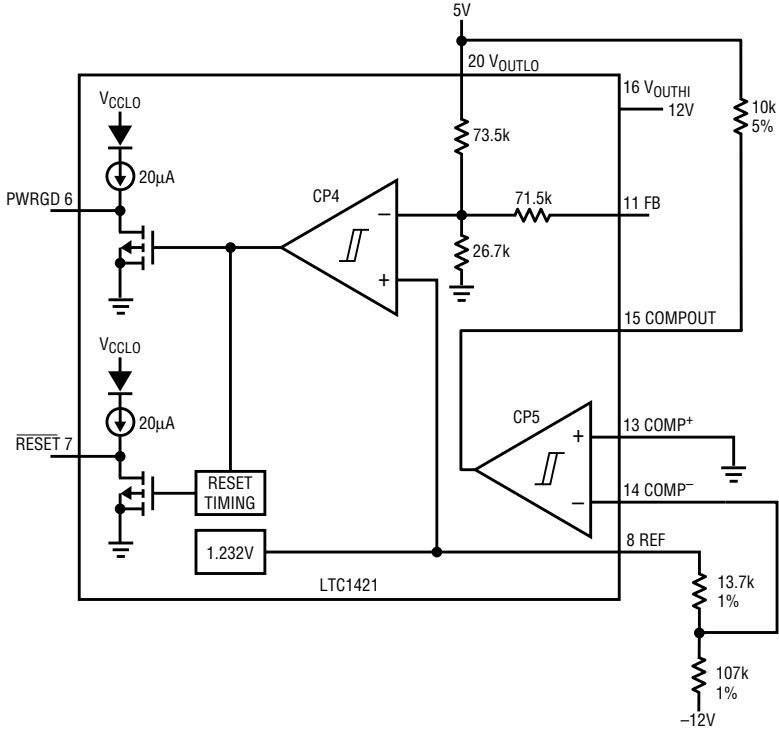
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Figure 7. CP5 can be used to monitor a negative supply voltage.
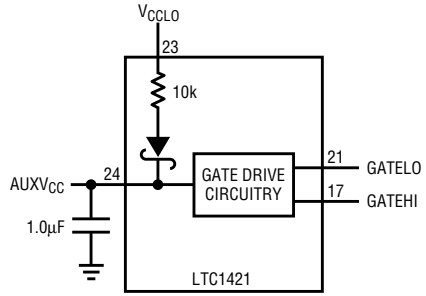
Figure 8. Auxiliary V_{CC} circuitry

Conclusion

With the explosion of systems requiring distributed power, the need for products that can be safely inserted into a live backplane has increased. Up to now, the design of the protection circuitry has required the talents of an analog guru, but with the LTC1421, safe hot swapping becomes as easy as hooking up an IC, a couple of power FETs and a handful of resistors and capacitors. *LT*

Figure 9. LTC1421 typical power-on reset cycle

The Care and Feeding of High Performance ADCs: Get All the Bits You Paid For

by William C. Rempfer

Introduction

A new generation of ADCs currently appearing on the scene brings higher performance and lower cost to new markets. Figure 1 shows an example of how high speed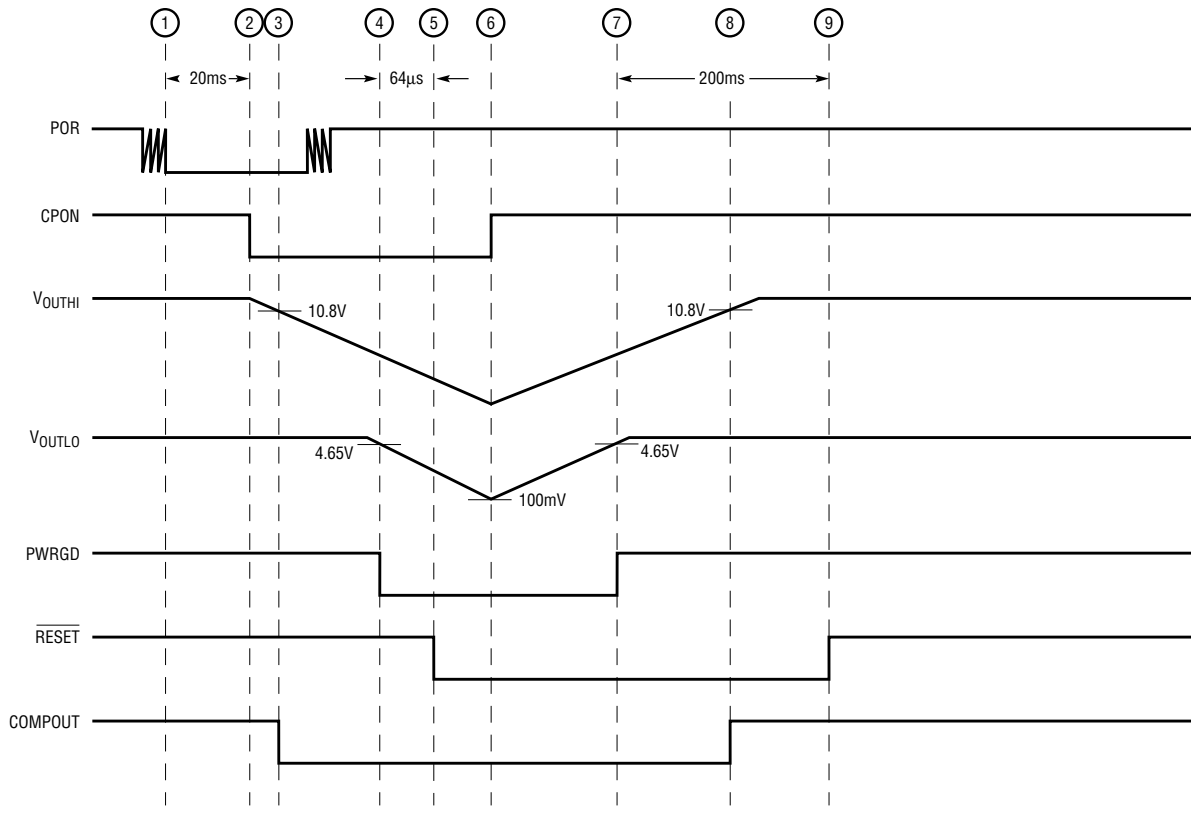 12-bit converters are becoming affordable for the first time to a new range of applications. At the same time, the new converters achieve better dynamic performance with high frequency input signals. All this means that more system designers are facing the challenge of using high performance ADCs. In this article, we will talk about some of the problems designers encounter, how to recognize their symptoms and how to avoid them. We will focus on the particular case of the LTC1410, a 1.25Msps, 12-bit ADC. The same considerations become important in higher resolution ADCs at lower speeds. Conversely, lower resolution ADCs will need this same attention at higher speeds.

An ADC Has Many Inputs

Providing a clean analog input signal to an ADC doesn't always guarantee a clean digital output signal. This is because an ADC has not just one input, but many. Ground pins, supply pins and reference pins also act as inputs and must be given special care to prevent noise and unwanted signals from corrupting the ADC output. Grounding, bypassing of the supplies and the reference and driving the analog and clock inputs are the major weapons in this battle against corruption.

Ground Planes and Grounding

Designing a high speed ADC system without using a proper ground is like trying to play basketball on a huge trampoline. No matter how well you mount the baskets to the court, the whole court will bounce and wobble as the players jump and try to shoot. To play the game, you must have a solid floor. Similarly, to give a solid ground for your data converter circuit, you must use an analog ground plane. This will put your circuit on a solid foundation.

Figure 2 shows grounding techniques for the LTC1410, a 1.25Msps, 12-bit ADC. This provides an example that can be modified for the particular high performance converter used. All bypass caps, reference caps and ground connections for the ADC should be tied to the analog ground plane. Tie them as close together as possible to reduce the sensitivity to currents that may flow in the ground plane. The input signal circuitry, filter caps and op amp bypass caps (not shown) should also be grounded to the ground plane near the ADC.

Noise from digital components in the system must be kept out of the analog ground. To do this, boards
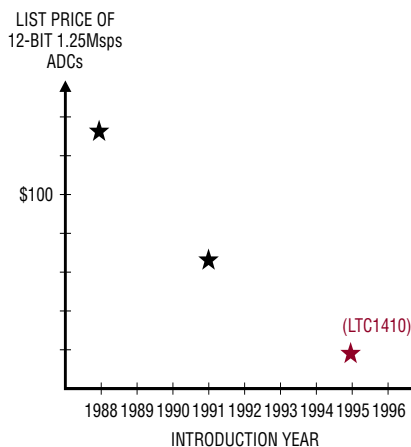
Figure 1. High performance 1.25Mbps, 12-bit ADCs are becoming affordable to a new range of applications. More system designers will need to know how to use them effectively.
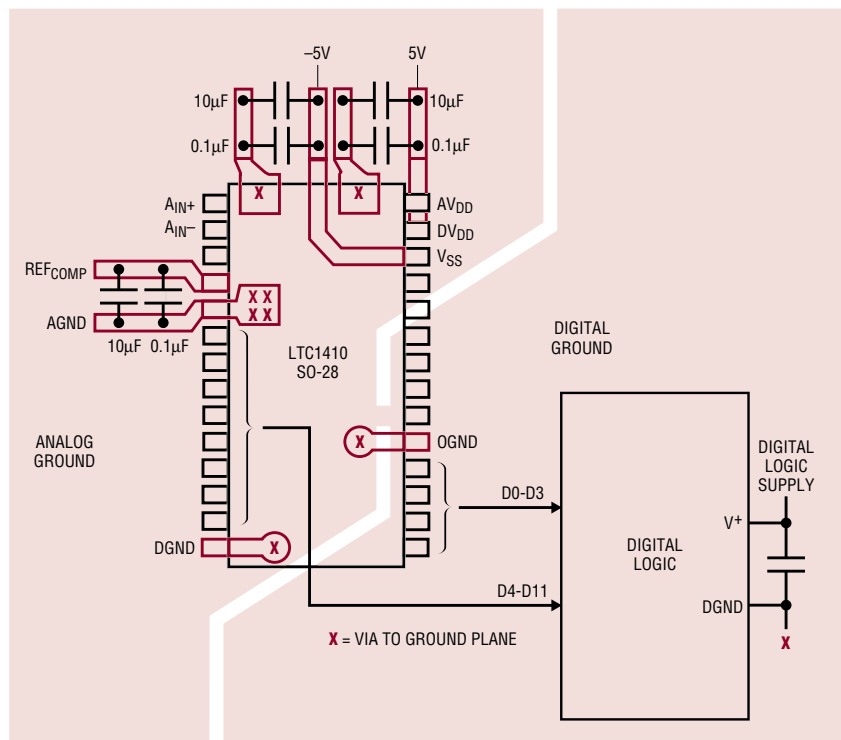
Figure 2. High performance ADC layout must have separate analog and digital ground planes, bypass caps with short connections and digital outputs routed away from the inputs.

should be designed with separate analog and digital ground planes, as shown in Figure 2. (The figure shows a 2-layer board layout. If more layers are available, separate layers may be used for analog and digital ground planes.) All noisy digital logic devices must be on the digital ground plane. All the grounds and bypass caps of the ADC (even the digital ones) should tie to the analog ground plane. Tie the two ground planes together at only one point to keep digital currents from taking shortcuts through the analog ground. The ideal connection point is the ground pin for the ADC output drivers (or the digital ground pin). If that is not possible, a different connection point can be used (for example, at the power supply). In any case, be sure to use only a single connection point.

Supply Bypassing

The high conversion rates of high performance converters require proper bypassing on the supply pins. The key to good bypassing is low lead inductance between the ADC and the bypass capacitors. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back through ground to the ground pin.

In Figure 2, the first components placed around the ADC are the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum $10\mu F$ surface mount devices are good if they are used in conjunction with $0.1\mu F$ ceramics. Even better are the new surface mount ceramic capacitors, which can be used alone. They come in values of $10\mu F$ or more and have ESR values as low as $20m\Omega$.

Figure 3a shows the differential nonlinearity (DNL) of the LTC1410 with good supply bypassing. Figure 3b shows the effects of 2 inches of lead length (corresponding to roughly 60nH of inductance) in series with the supply bypass caps. This is an exaggerated case of poor bypassing layout, which causes the DNL to de-
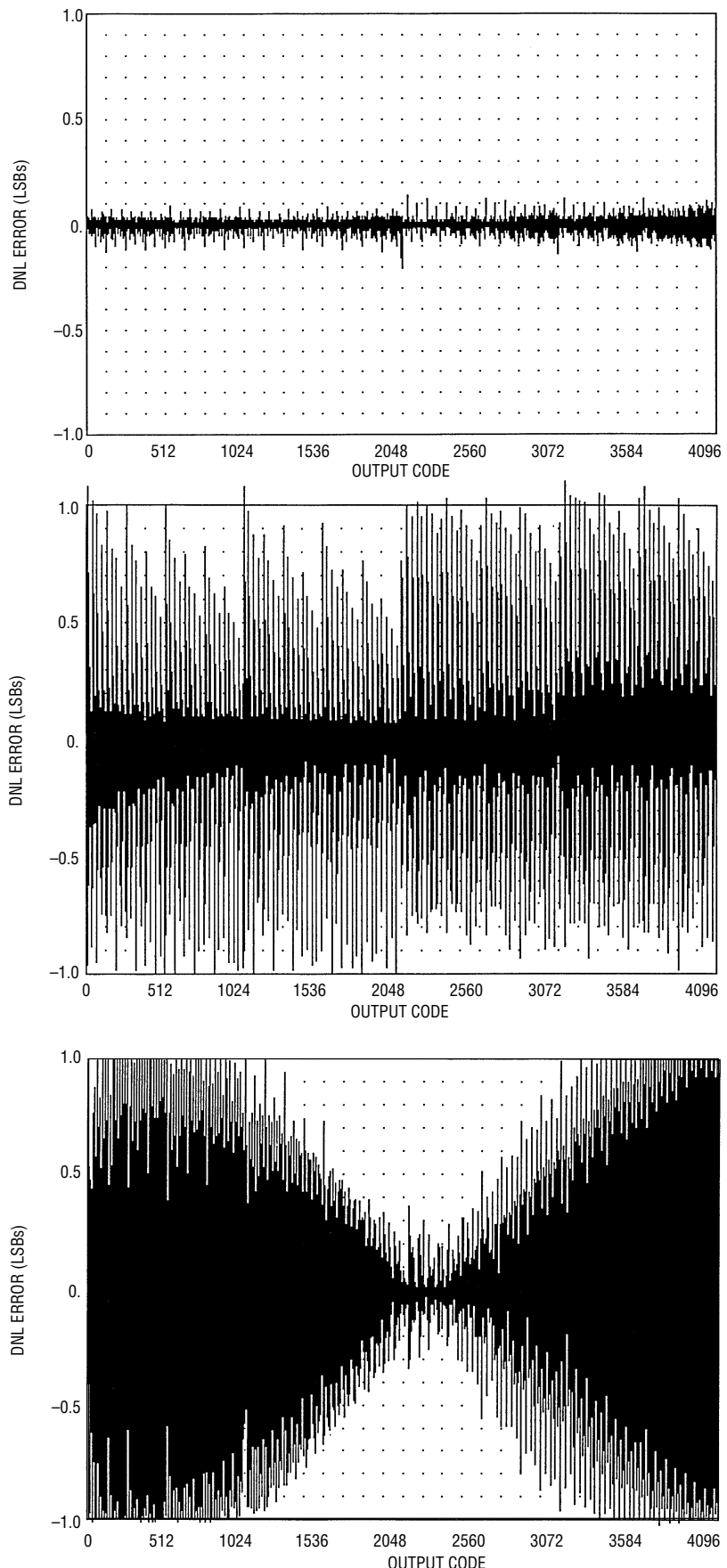
Figure 3. Poor layout will degrade the differential nonlinearity (DNL) of fast ADCs: a. (top) a clean LTC1410 layout with bypass cap wires of less than 0.5 inch; b. (middle) 2-inch wires to supply-bypass caps; c. (bottom) a wire of more than 2 inches to the reference-bypass cap.

grade beyond 1LSB, reducing the accuracy to 11 bits. For best performance, use supply bypass leads of less than one-half inch. A little care pays off with excellent performance.

Reference Bypassing

The analog reference input provides the scale factor for the conversion. For a clean data output the reference must be stable. Dynamic currents pulled from the reference by the ADC as it converts perturb the reference unless it is properly bypassed. Surface mount tantalum or ceramic capacitors provide good results. They should be located near the reference pin and should be grounded very near the ADC analog ground pin, as shown in Figure 2.

Figure 3c shows the easily recognizable signature of a reference bypassing problem—a bow-tie shape to the error curve. This occurs because reference perturbations feed in with full strength for inputs near plus or minus full scale but have less effect for inputs near zero scale. This degradation in DNL results from several inches of lead length in series with the reference bypass cap. Once again, this is an exaggerated case to make the consequences of poor bypassing more visible. To maintain high accuracy, keep the lead lengths less than half an inch.

Driving the Analog Input

Switched Capacitor Inputs

The inputs to switched capacitor ADCs are easy to drive if you allow for the fact that they draw a small input-current transient at the end of each conversion. This happens when the internal sampling capacitors switch back onto the input to acquire the next sample. For accurate results, the circuitry driving the analog input must settle from this transient before the next conversion is started.

There are two ways to accomplish this. One is to drive the ADC with an op amp that settles from a load transient in less than the acquisition time of the ADC. Fortunately, most op amps settle much more quickly from

a load transient than from an input step, so meeting this requirement is not too difficult. The LT1363, for example, is a good choice for driving the LTC1410 input.

A second solution to handling the input transient is to use an input RC filter with a capacitor much larger than the ADC input capacitance. This larger capacitor provides the charge for the sampling capacitor, which eliminates the voltage transient altogether. Figure 4 shows such a filter for the LTC1410. The 1000pF capacitor provides the input charge for the ADC's sampling capacitor. The LT1363's capacitive load driving capability makes it a good choice for use with this filter.

Filter Wideband Noise from the Input Signal

Many new converters have wide S/H input bandwidths. This is great for capturing high frequency input signals, but for lower input bandwidth applications the converter will pick up any wideband noise that may be in the input signal. To avoid this, use a filter at the ADC input to pass only your desired signal bandwidth.

The simple filter in Figure 4 bandlimits the input signal to 3MHz and still allows clean sampling up to the Nyquist frequency (625kHz). Figure 7a shows the Nyquist performance of the LTC1410 using this filter. The signal to noise and distortion ratio (SINAD) is 71.5dB and total harmonic distortion (THD) is –84dB.

Choosing an Op Amp

To drive high performance ADCs, you will need a high performance op amp.

The noise and distortion of good ADCs are now so low that they no longer mask the performance of the op amp. This adds another tradeoff to op amp selection.

High speed, current feedback op amps have lower DC precision and don't settle as well to high accuracy (for example, 0.01%) as the voltage feedback types. However, they have the best distortion and drive for high speed AC frequency domain applications. Figure 5a shows the FFT result of an LT1227 current feedback amp driving a 172kHz signal into the LTC1410. The distortion (THD) of –82dB is about 3dB worse than the –85dB of the ADC alone.

High speed voltage feedback amplifiers have better precision and settling. They work well in frequency domain applications but are best suited for high speed, time domain or multiplexed applications where their DC precision and settling are required. Figure 5b shows the voltage feedback LT1363's 2dB further degradation in distortion (to –80dB) under the same conditions.

Slower op amps like the OP-27/ OP-37 are excellent in noise and precision but are simply not fast enough for high frequency applications. They distort as they are pushed beyond their slewing capabilities (as shown in the FFT plot of Figure 5c).

Driving the Convert-Start Input

An improperly driven conversion-start input can create conversion errors in a couple of ways. First, if an ADC has internal timing, the returning edge of the convert signal (the opposite edge
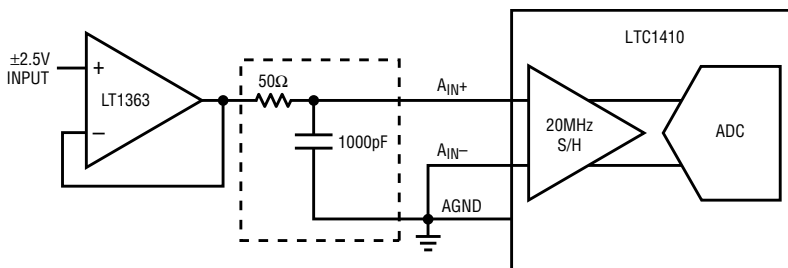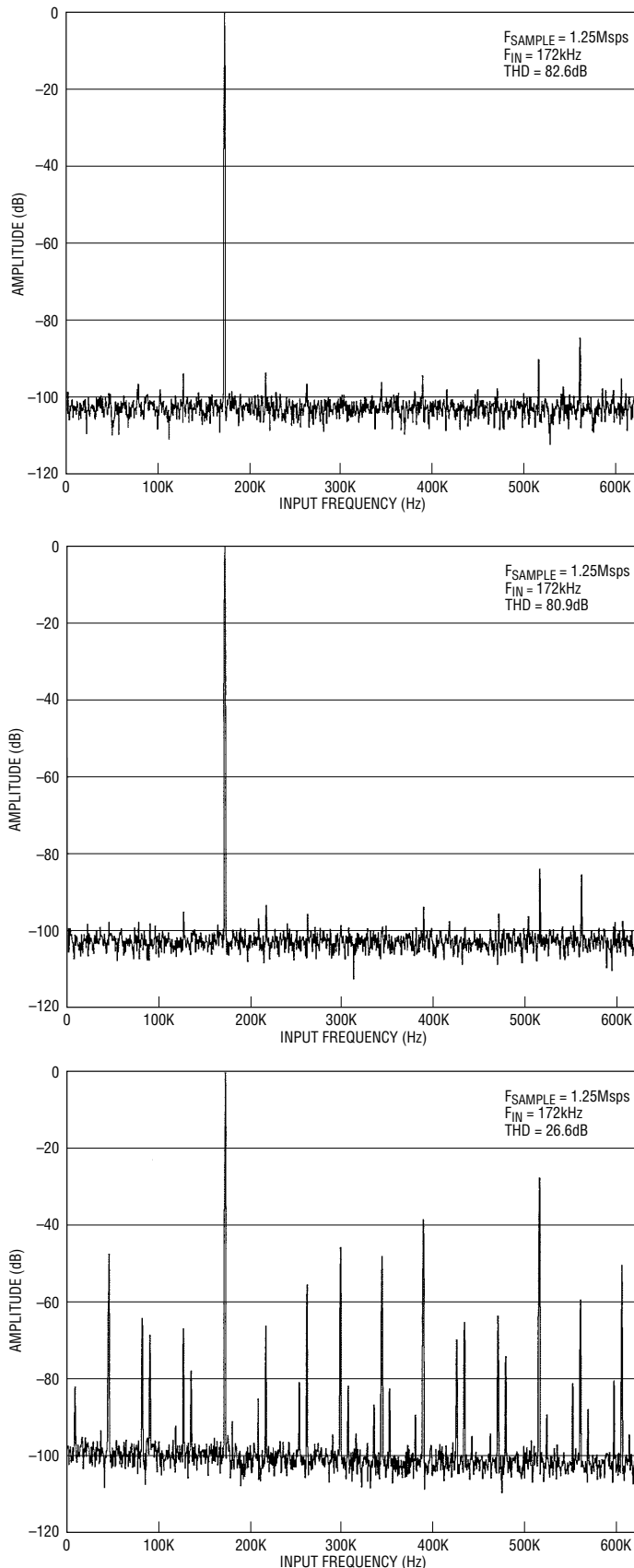

Figure 4. Many new ADCs have wide-bandwidth sample-and-holds. In lower bandwidth applications, a simple RC filter will remove wideband noise that may be present in the input signal.

Figure 5. Op amp selection is important when an ADC has low distortion levels. a. (top) Current feedback op amps such as the LT1227 (seen here driving the LTC1410) provide the lowest THD in the FFT output; b. (middle) Fast voltage feedback op amps do nearly as well in THD as current feedback amps and offer better precision; c. (bottom) slower op amps pushed beyond their slew limits will severely distort fast signals.

from the one that starts the conversion) can couple noise into the converter if it occurs during the conversion time. To avoid this, use a narrow pulse for convert-start instead of a square wave. This ensures that it either returns quickly (after the sample is taken but before the conversion gets underway), or returns after the conversion is over. (This does not apply to those ADCs that draw all their timing from a clock input and require precise 50% duty-cycle clock inputs.)

A convert-start signal that overshoots or rings can also degrade performance. If it overshoots beyond the supply rails it can turn on the ADC's input protection diodes and couple noise into the converter. If it rings, it may still be bouncing around as the ADC's sample-and-hold captures the input signal, which can affect the conversion result. Normally, overshoot and ringing are not a problem with high speed CMOS logic on a well designed board but they are still things to watch out for.

High frequency or high slew rate input signals impose another requirement on the ADC: low aperture jitter. Aperture jitter is the variation in the ADC's aperture delay from conversion to conversion and results in an uncertainty in the time when the input sample is taken. Figure 6 shows how this jitter causes an equivalent input noise by working against the slew rate of the analog input signal. The faster the input signal slew rate, the worse the noise for a given jitter. The best possible SINAD for an ADC is limited by the jitter according to the formula:

$$SINAD(dB) \leq 20log[1/(2\pi \times t_{JITTER(RMS)} \times f_{INPUT})]$$

where:

$t_{JITTER(RMS)}$ = the RMS jitter in seconds

f_{INPUT} = the analog input frequency in Hz

The LTC1410's 5ps (RMS) aperture jitter allows clean sampling of inputs far beyond the Nyquist frequency. However, to achieve this performance, the convert-start input signal applied to the ADC must also have low jitter. Figure 7a shows the

ADC, driven from a low jitter source, capturing a 600kHz input with 71.5dB SINAD. As Figure 7b shows, adding 70ps of jitter to the conversion-start input signal will raise the noise floor, and reduce the SINAD, by 3dB.

If generating a lower jitter signal is a problem, one trick is to start with a higher frequency clock, which will usually have lower jitter, and then divide the frequency down with fast logic (which retains the lower jitter) to get the desired sample clock.

Routing the Data Outputs

One of the worst potential sources of digital noise and coupling in an ADC is its output data bus. Fortunately, the user can control this with proper board layout. First, to prevent the data outputs of the ADC from capacitively coupling to the analog input circuitry, they should be routed in the opposite direction. This will naturally occur if separate digital and analog ground plane layouts are used, as in Figure 2. Second, the digital
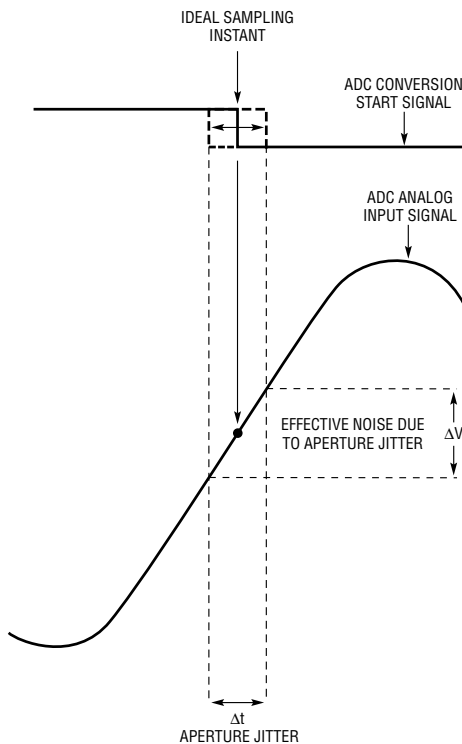
Figure 6. Aperture jitter in a sampling ADC or jitter in the conversion-start signal applied to the ADC can degrade its noise performance. The time jitter works against the slope of the analog input signal to generate an effective noise voltage that appears in the ADC's output spectrum.
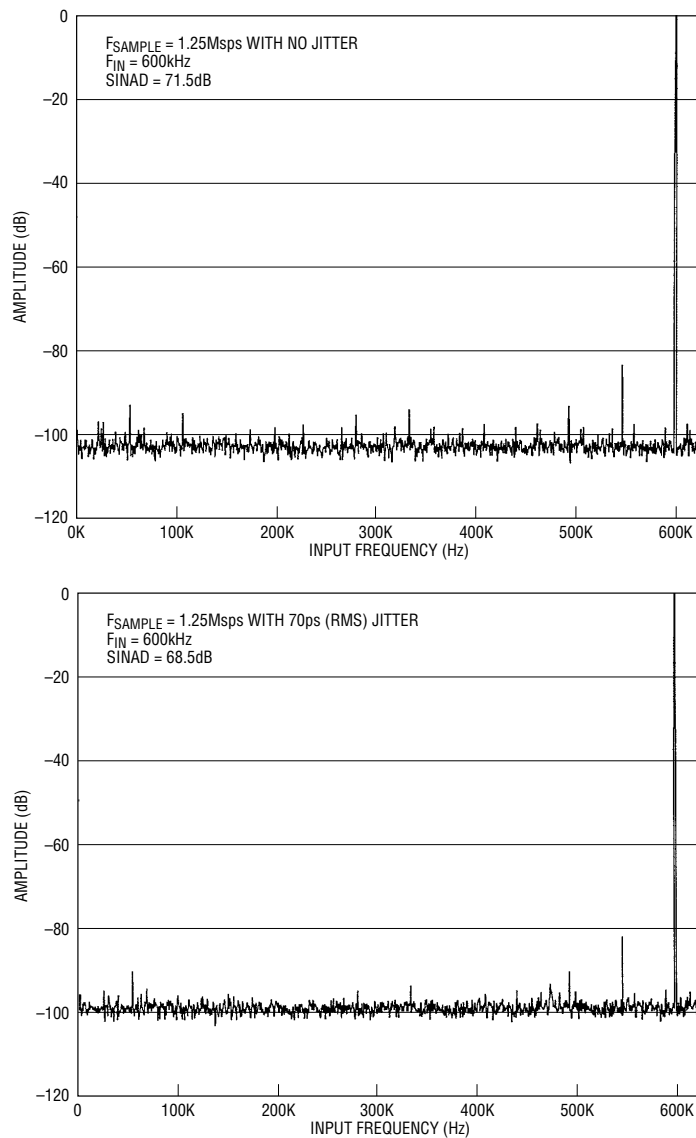
Figure 7. Jitter in the conversion signal creates noise: a. (top) with a low jitter source, the LTC1410 will give 71.5dB SINAD when sampling a Nyquist input signal; b. (bottom) adding 70ps of jitter to the convert-start signal will raise the noise floor by 3dB to 68.5dB.

output drivers in the ADC switch quickly and will create large current transients if they are loaded with too much capacitance. Locating the receiving buffers or latches close to the ADC will minimize loading.

Although reduced, some capacitive currents still flow, and it is important to control their return path to the driver of the ADC. Starting from the output drivers of the ADC, the current goes through the output lines, charges the input capacitance of the receiving latches or buffers, and returns through the digital ground plane to the ADC's output driver. For a falling edge, this current returns

into the output driver ground pin. For a rising edge, it returns to the ground point of the output driver's supply-bypass cap. Tying the digital and analog grounds together at the ADC output driver ground pin (as in Figure 2) helps prevent this current from flowing across the analog ground plane. If the grounds must be tied at the power supply instead of at the ADC, the return currents will flow through the analog ground plane. In this case, it is especially important to minimize these currents by minimizing the capacitance on the digital outputs. *⌐⊅*

LTC1433/LTC1434:
High Efficiency, Constant-Frequency
Monolithic Buck Converter by San-Hwa Chee

Introduction

In portable communications products where high efficiency and constant frequency operation are prime requirements, the LTC1433 and LTC1434 are a perfect fit. These two new devices are packed with features but still fit in a small footprint. The LTC1433 comes in a 16-pin narrow SSOP, whereas the LTC1434 comes in a 20-pin narrow SSOP. The LTC1434 provides an additional feature that allows the device to be synchronized with an external clock through its internal PLL.

High efficiency and constant frequency at low load current are achieved by using the new Adaptive Power™ output stage, first introduced in the LTC1435–LTC1439 DC/DC controllers ("New LTC1435–LT1439 DC/DC Controllers Feature Value and Performance"; *Linear Technology* VI:1 (February 1996)). The LTC1433 and LTC1434 combine Adaptive Power operation with internal power MOSFETs for the first time, with operating frequency programmable up to 500kHz by means of a single external capacitor.

With no load, the devices require only 470µA of quiescent current, which drops to 15µA in full shutdown. In dropout conditions, the internal 0.6Ω (at an input supply of 10V) power P-channel MOSFET switch is turned on continuously (DC), thereby maximizing the life of the battery source. In the event of an output short circuit, the oscillator frequency is reduced by a factor of 4.5 to prevent inductor-current runaway. In addition, an internal sense resistor limits the switch current to 1.2A.

Both devices contain a low-battery detector and a power-on reset (POR) timer that generates a signal delayed by 65,536 oscillator clock cycles after the output is within 5% of regulated output voltage. A soft-start pin allows the LTC1433/LTC1434 to power up gently and also serves as a shutdown pin. For maximum flexibility, internal resistive feedback dividers are selectable via programming pins for 3.3V or 5V, or can be configured with an adjustable output voltage to meet any requirement. Both devices function down to an input voltage of 3.5V and up to an absolute maximum of 13.5V.

What is Adaptive Power Mode Operation?

The LTC1433/LTC1434 have two internal P-channel MOSFETs of different sizes, with each drain bonded out separately. To maximize efficiency, only the smaller sized P-channel MOSFET is switched on and off at low load currents. This reduces gate-charge losses without changing the operating frequency. At higher load currents, both MOSFETs are switched, since losses due to drops across the FETs are more significant than gate-charge losses. The
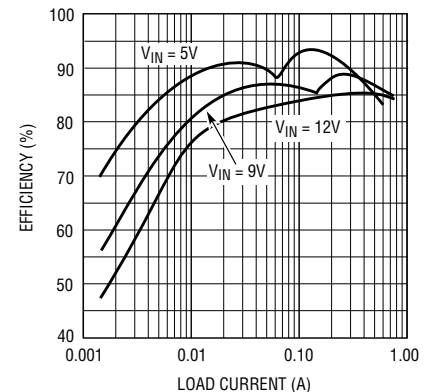
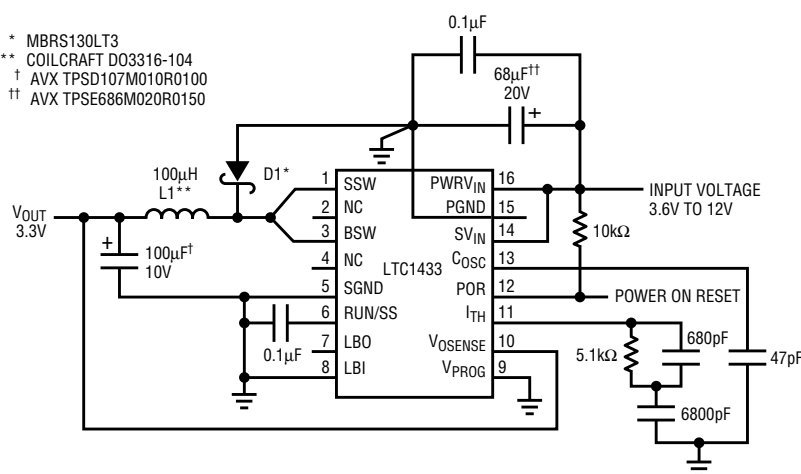**Figure 2. Efficiency versus load current for Figure 1's circuit**

Figure 3. Single-inductor configuration
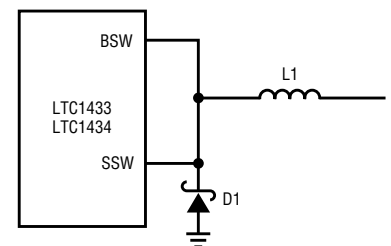
Figure 1. Typical application using the LTC1433

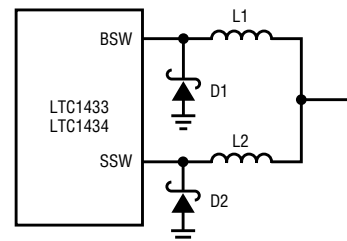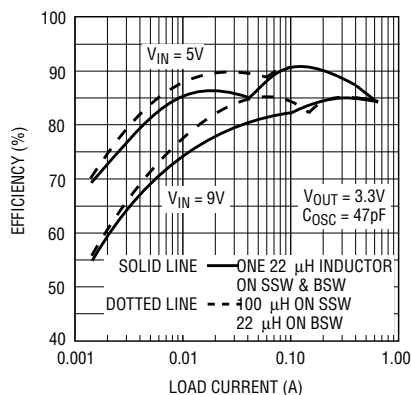**Figure 4. Dual-inductor configuration**

Figure 5. Efficiency comparison between single- and dual-inductor configurations

Figure 6. Dropout characteristics at different load currents for $V_{OUT} = 3.3V$

Figure 7. Dropout characteristics at different load currents for $V_{OUT} = 5.0V$

LTC1433/LTC1434 monitor two conditions to determine when to switch to low current mode: inductor current and error amplifier output voltage (on the I_{TH} pin). If the peak current of the inductor does not exceed 260mA and the voltage at the I_{TH} pin does not exceed 0.6V, the small MOSFET will be used. When either one of the conditions is exceeded, the large MOSFET will be used on the next clock cycle.

Efficiency

Figure 1 shows a practical LTC1433 circuit that can be used for cellular telephone applications. Efficiency curves for this circuit at various input voltages are shown in Figure 2. Note that the efficiency reaches 93% at a supply voltage of 5V and a load current of about 150mA. This high efficiency makes the LTC1433 and LTC1434 attractive for all other power-sensitive applications. The circuit
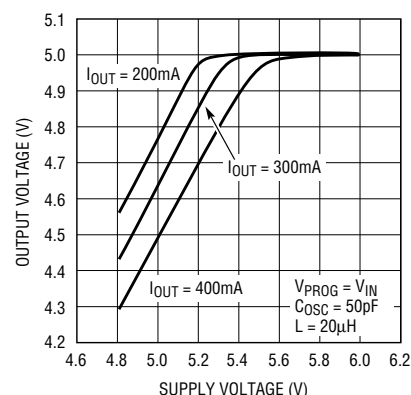
works all the way down to 3.6V at a load current of 250mA before dropping out and the oscillator frequency is a constant 210kHz down to 20mA load current.

Efficiency Considerations

Since there are two separate pins for the drains of the small and large P-channel switches, we could use two inductors to further enhance the efficiency of the regulator over the low current range. Figures 3 and 4 show the single-inductor and dual-inductor circuit configurations, respectively. To reduce core losses, a higher value inductor can be used on the small P-channel switch. Since this switch only carries a small part of the overall current, the user can still specify a small physical size inductor without sacrificing on copper losses. The Schottky on the small P-channel drain (SSW) can also be chosen with a lower

current rating. As can be seen from Figure 5, the average efficiency gain over the region where the small P-channel is ON is about 3%. Hence, the dual inductor configuration is good for applications that require maximum efficiency at low load currents, while retaining constant-frequency operation.

100% Duty Cycle in Dropout

When the input voltage decreases, the inductor's ripple current starts to decrease and the duty cycle increases to provide the required output current. Further decrease in input voltage will eventually cause the I_{TH} voltage to be at its maximum limit. Any decrease in input voltage from this point will result in the P-channel switch being turned on continuously. The dropout voltage, $V_{IN} - V_{OUT}$, is governed by the switch resistance, load current and the voltage drop across

* MOTOROLA MBRS130LT3
** COILCRAFT DO3316 SERIES
† AVX TPSD107M010R0100
†† AVX TPSE107M016R0100

V_{IN} (V)	$I_{OUT\ MAX}$ (mA)
3.0	180
4.0	240
5.0	290
6.0	340
7.0	410
7.5	420
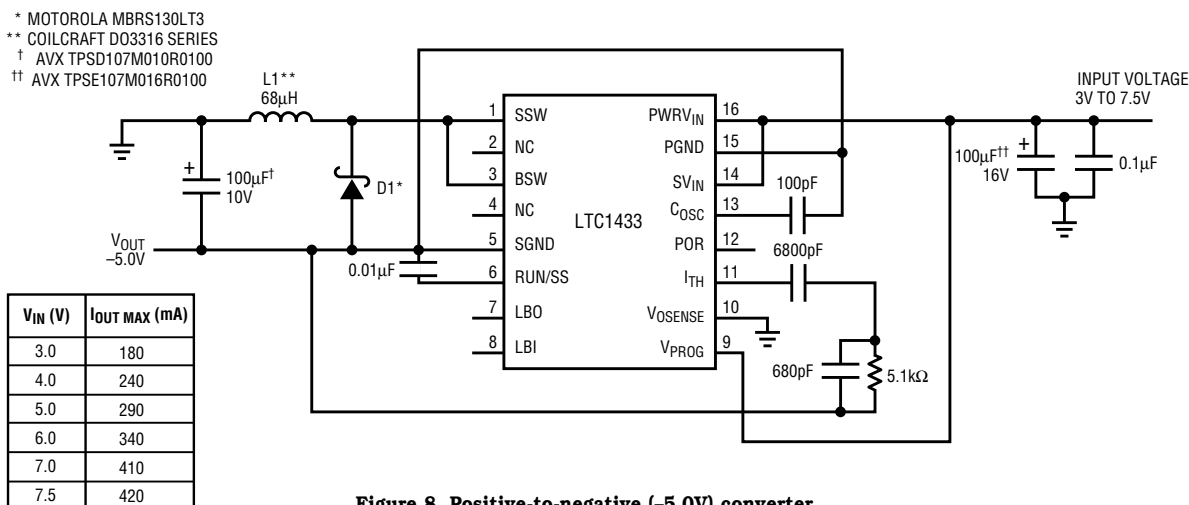
Figure 8. Positive-to-negative (–5.0V) converter

The LTC1343 and LTC1344 Form a Software-Selectable Multiple-Protocol Interface Port Using a DB-25 Connector

by Robert Reay

Introduction

With the explosive growth in data networking equipment has come the need to support many different serial protocols using only one connector. The problem facing interface designers is to make the circuitry for each serial protocol share the same connector pins without introducing conflicts. The main source of frustration is that each serial protocol requires a different line termination that is not easily or cheaply switched.

With the introduction of the LTC1343 and LTC1344, a complete software-selectable serial interface port using an inexpensive DB-25 connector becomes possible. The chips form a serial interface port that supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode

and is both NET1 and NET2 compliant. The port runs from a single 5V supply and supports an echoed clock and loop-back configuration that helps eliminate glue logic between the serial controller and the line transceivers.

A typical application is shown in Figure 1. Two LTC1343s and one LTC1344 form the interface port using a DB-25 connector, shown here in DTE mode.

Each LTC1343 contains four drivers and four receivers and the LTC1344 contains six switchable resistive terminators. The first LTC1343 is connected to the clock and data signal lines along with the diagnostic LL (local loop-back) and TM (test mode) signals. The second LTC1343 is connected to the control-

signal lines along with the diagnostic RL (remote loop-back) signal. The single-ended driver and receiver could be separated to support the RI (ring-indicate) signal. The switchable line terminators in the LTC1344 are connected only to the high speed clock and data signals. When the interface protocol is changed via the digital mode selection pins (not shown), the drivers and receivers are automatically reconfigured and the appropriate line terminators are connected.

Review of Interface Standards

The serial interface standards RS232, EIA-530, EIA-530A, RS449, V.35, V.36 and X.21 specify the function of each signal line, the electrical characteristics of each signal, the connector type,
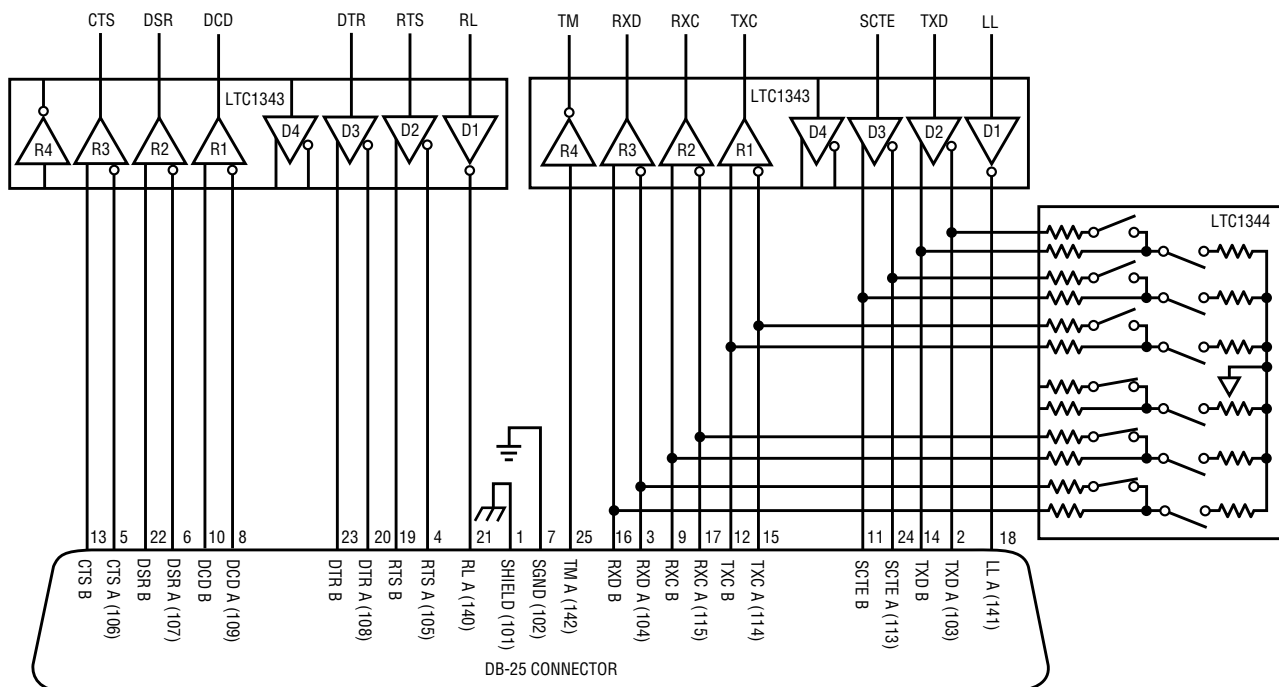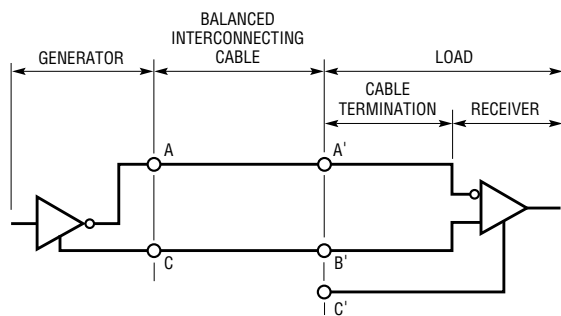

Figure 1. LTC1343/LTC1344 typical application

Figure 2. Typical V.10 interface

Figure 3. V.10 receiver configuration

the transmission rate and the data exchange protocols. The RS422 (V.11) and RS423 (V.10) standards merely define electrical characteristics. The RS232 (V.28) and V.35 standards also specify their own electrical characteristics. In general, the US standards start with RS or EIA, and the equivalent European standards start with V or X. The characteristics of each interface are summarized in Table 1.

Table 1 shows only the most commonly used signal lines. Note that each signal line must conform to only one of four electrical standards, V.10, V.11, V.28 or V.35.
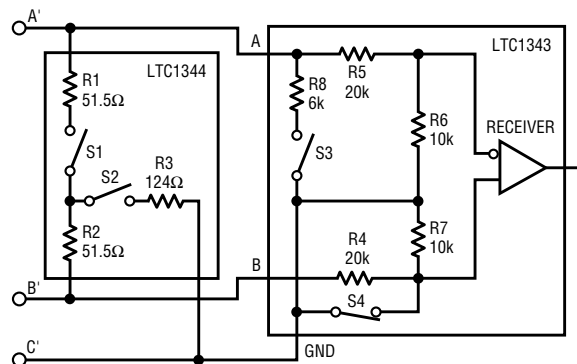
V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 2. A V.10 single-ended generator (output A with ground C) is connected to a differential receiver with input A' connected to A and input B' connected to the signal-return ground C. The receiver's

ground C' is separate from the signal return. Usually, no cable termination between A' and B' is required for V.10 interfaces. The V.10 receiver configuration for the LTC1343 and LTC1344 is shown in Figure 3.

> *With the introduction of the LTC1343 and LTC1344, a complete software-selectable serial interface port using an inexpensive DB-25 connector becomes possible. The chips form a serial interface port that supports a wide variety of standards.*

In V.10 mode, switches S1 and S2 inside the LTC1344 and S3 inside the LTC1343 are turned off. Switch S4 inside the LTC1343 shorts the noninverting receiver input to ground so

the B input at the connector can be left floating. The cable termination is then the 30k input impedance to the ground of the LTC1343 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 4. A V.11 differential generator with outputs A and B and ground C is connected to a differential receiver with ground C', input A' connected to A and input B' connected to B. The V.11 interface has a differential termination at the receiver end with a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. In V.11 mode, all switches are off except S1 inside the LTC1344, which connects a 103Ω differential termination impedance to the cable, as shown in Figure 5.

Table 1. Interface summary

|	Clock and Data Signals					Control Signals					Test Signals			
	TXD	SCTE	TXC	RXC	RXD	RTS	DTR	DSR	DCD	CTS	RI	LL	RL	TM
CCITT#	(103)	(113)	(114)	(115)	(104)	(105)	(108)	(107)	(109)	(106)	(125)	(141)	(140)	(142)
RS232	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
EIA-530	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	—	V.10	V.10	V.10
EIA-530A	V.11	V.11	V.11	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.10	V.10	V.10	V.10
RS449	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.10	V.10	V.10	V.10
V.35	V.35	V.35	V.35	V.35	V.35	V.28	—	V.28	V.28	V.28	—	—	—	—
V.36	V.11	V.11	V.11	V.11	V.11	V.11	—	V.11	V.11	V.11	—	V.10	V.10	V.10
X.21	V.11	V.11	V.11	V.11	V.11	V.11	—	—	V.11	—	—	—	—	—
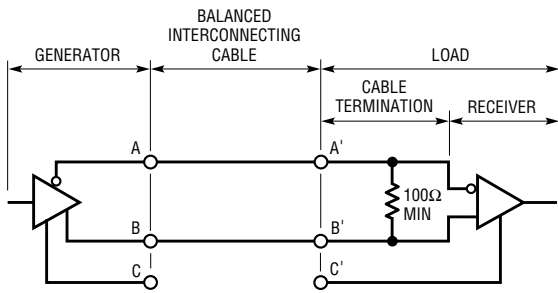
Figure 4. Typical V.11 interface
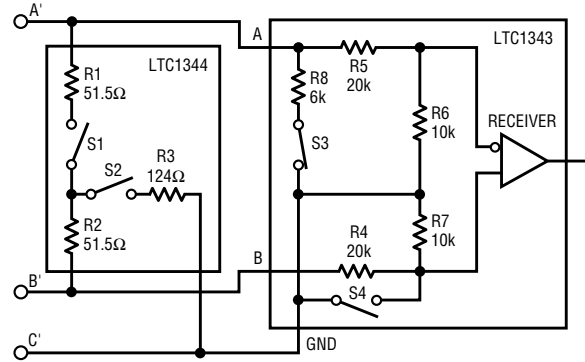
Figure 7. V.28 receiver configuration
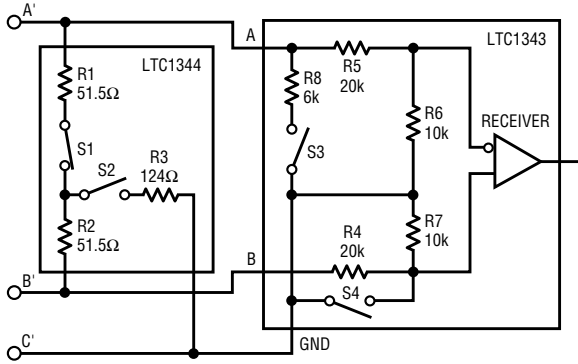

Figure 5. V.11 receiver configuration
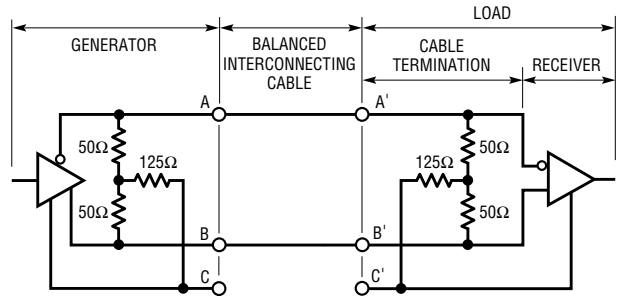
Figure 8. Typical V.35 interface

Figure 6. Typical V.28 interface

Figure 9. V.35 receiver configuration

Table 2. LTC1343/LTC1344 mode selection

LTC1343 Mode Name	M2	M1	M0	CTRL/ $\overline{CLK}$	D1	D 2	D 3	D 4	R1	R 2	R 3	R 4
V.10/RS423	0	0	0	X	V.10	V.10	V.10	V.10	V.10	V.10	V.10	V.10
RS530A clock & data	0	0	1	0	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
RS530A control	0	0	1	1	V.10	V.11	V.10	V.11	V.11	V.10	V.11	V.10
Reserved	0	1	0	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
X.21	0	1	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.35 clock & data	1	0	0	0	V.28	V.35	V.35	V.35	V.35	V.35	V.35	V.28
V.35 control	1	0	0	1	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
RS530/RS449/V.36	1	0	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.28/RS232	1	1	0	X	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
No Cable	1	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z
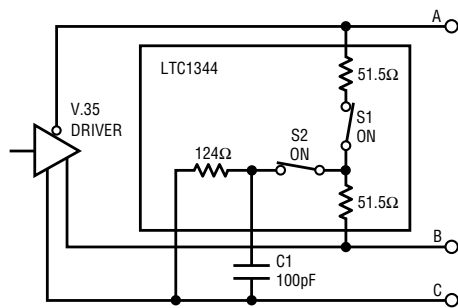
Figure 10. V.35 driver using the LTC1344

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 6. A V.28 single-ended generator (output A with ground C) is connected to a single-ended receiver with input A' connected to A and ground C' connected via the signal return ground to C. In V.28 mode, all switches are off except S3 inside the LTC1343, which connects a 6k impedance (R8) to ground in parallel with 20k (R5) plus 10k (R6), for an combined impedance of 5k, as shown in Figure 7. The noninverting input is disconnected inside the LTC1343 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

V.35 Interface

A typical V.35 balanced interface is shown in Figure 8. A V.35 differential generator with outputs A and B and ground C is connected to a differential receiver with ground C', input A' connected to A and input B' connected to B. The V.35 interface requires T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100 ±10Ω, and the impedance between shorted terminals (A' and B') and ground (C') is 150 ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1344 are on, connecting the T-network impedance, as shown in Figure 9. Both switches in the LTC1343 are off. The 30k input impedance of the receiver is placed in parallel with the T-network termination, but does not affect the overall input impedance significantly.
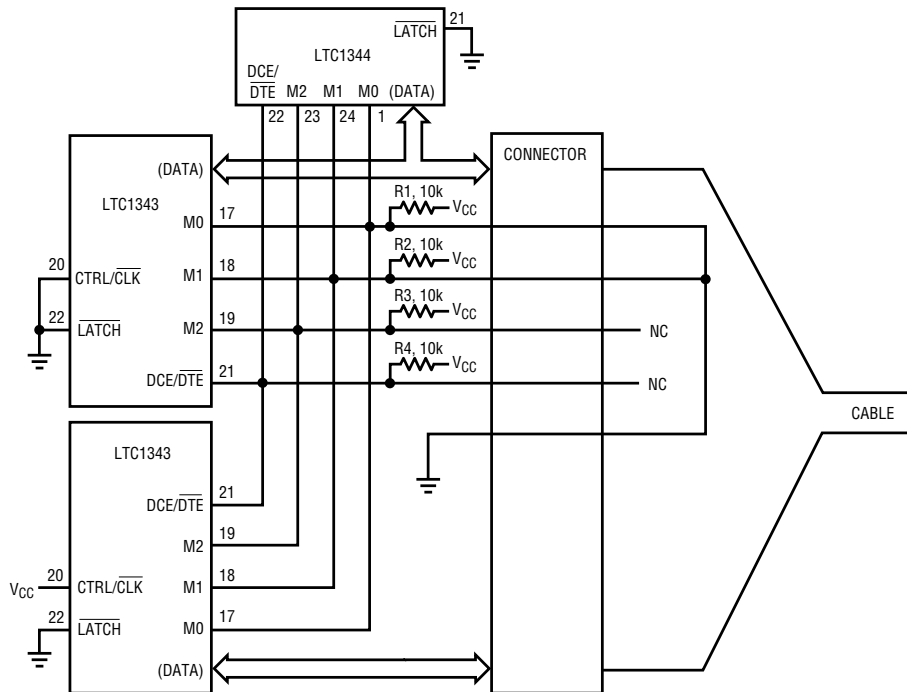
Figure 11. Mode selection by cable
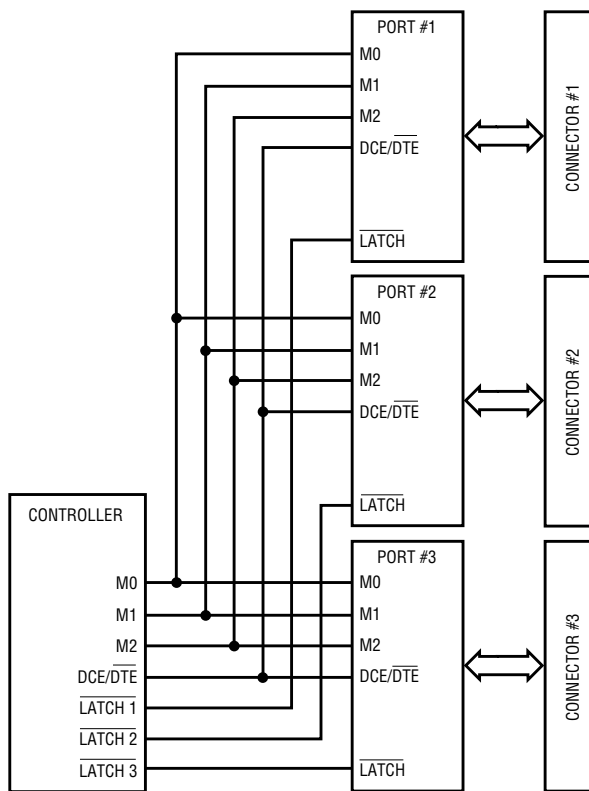
Figure 12. Mode selection by controller
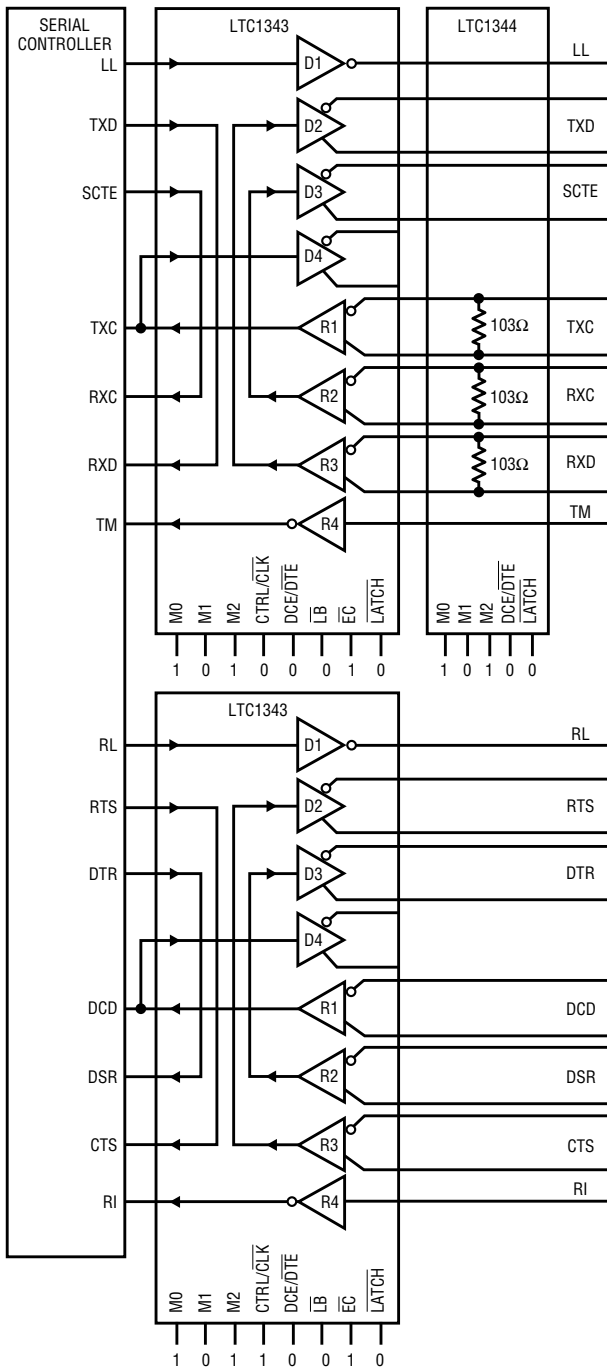
Figure 13. Normal DTE Loop-back
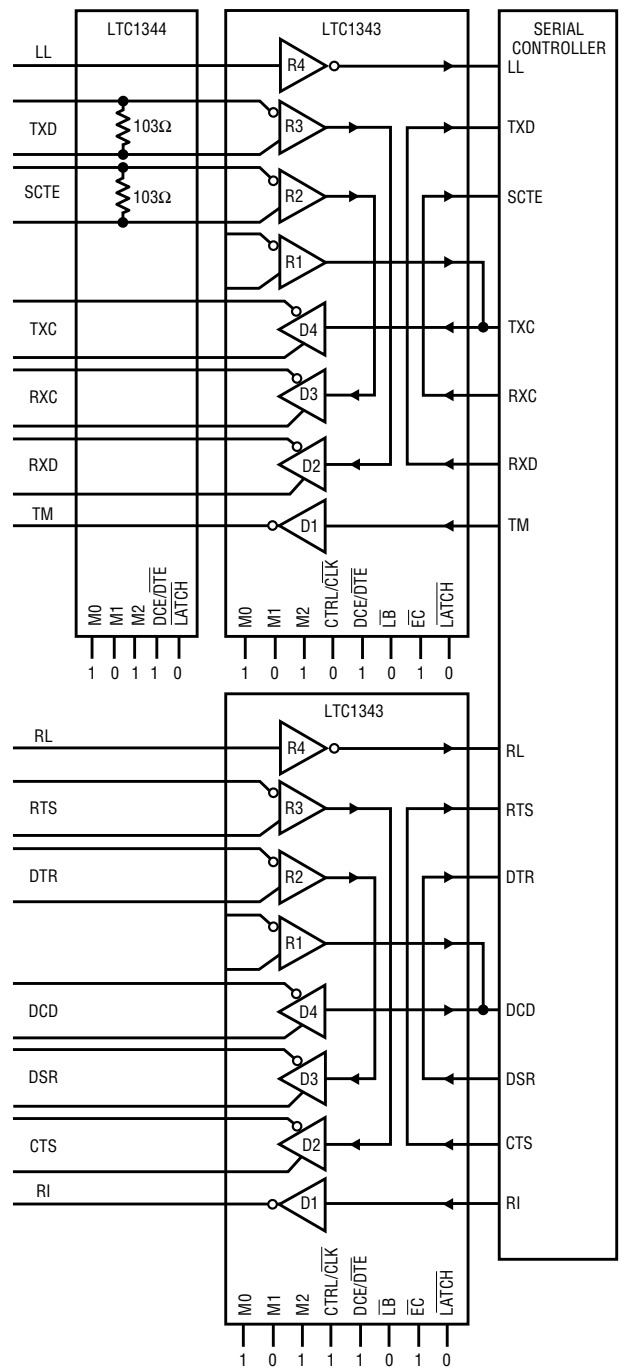
Figure 14. Normal DCE loop-back

The generator differential impedance must be 50Ω to 150Ω, and the impedance between shorted terminals (A and B) and ground (C) is 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise, as shown in Figure 10.

Any mismatch in the driver rise and fall times or skew in driver propagation delays will force current through the center termination resistor to ground, causing a high frequency common mode spike on the A and B terminals. This spike can cause EMI problems that are reduced by capacitor C1, which shunts much of the common mode energy to ground rather than down the cable.

LTC1343/LTC1344 Mode Selection

The interface protocol is selected using the mode select pins M0, M1, M2 and CTRL/$\overline{\text{CLK}}$, as summarized in Table 2. The CTRL/$\overline{\text{CLK}}$ pin should be pulled high if the LTC1343 is being used to generate control signals and pulled low if used to generate clock and data signals.

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, CTRL/$\overline{CLK}$ = 1 and the drivers and receivers will operate in RS232 (V.28) electrical mode. For the clock and data signals, CTRL/$\overline{CLK}$ = 0 and the drivers and receivers will operate in V.35 electrical mode, except for the single-ended driver and receiver, which will operate in the RS232 (V.28) electrical mode. The DCE/$\overline{DTE}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected by simply plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable, as shown in Figure 11.

The pull-up resistors R1–R4 ensure a binary 1 when a pin is left unconnected and also ensure that the two LTC1343s and the LTC1344 enter the no-cable mode when the cable is removed. In the no-cable mode, the LTC1343 power supply current drops to less than 200µA and all LTC1343 driver outputs and LTC1344 resistive terminators are forced into a high impedance state. Note that the data latch pin, $\overline{LATCH}$, is shorted to ground for all chips.

The interface protocol may also be selected by the serial controller or host microprocessor, as shown in Figure 12.

The mode selection pins M0, M1, M2 and DCE/$\overline{DTE}$ can be shared among multiple interface ports, while each port has a unique data-latch signal that acts as a write enable. When the $\overline{LATCH}$ pin is low, the buffers on the M0, M1, M2, CTRL/$\overline{CLK}$, DCE/$\overline{DTE}$, LB and $\overline{EC}$ pins are transparent. When the $\overline{LATCH}$ pin is pulled high, the buffers latch the data, and changes on the input pins will no longer affect the chip.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.
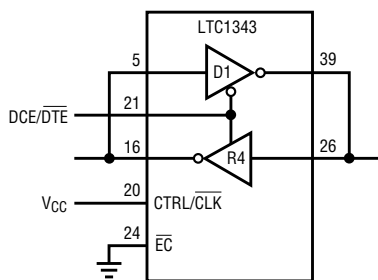
Figure 15. Single-ended driver and receiver enable

Loop-Back

The LTC1343 contains logic for placing the interface into a loop-back configuration for testing. Both DTE and DCE loop-back configurations are supported. Figure 13 shows a complete DTE interface in the loop-back configuration and Figure 14 the DCE loop-back configuration. The loop-back configuration is selected by pulling the $\overline{LB}$ pin low.

Enabling the Single-Ended Driver and Receiver

When the LTC1343 is being used to generate the control signals (CTRL/$\overline{CLK}$ = high) and the $\overline{EC}$ pin is pulled low, the DCE/$\overline{DTE}$ pin becomes an enable for driver 1 and receiver 4 so their inputs and outputs can be tied together, as shown in Figure 15.

The EC pin has no affect on the configuration when CTRL/$\overline{CLK}$ is high except to allow the DCE/$\overline{DTE}$ pin to become an enable. When DCE/$\overline{DTE}$ is low, the driver 1 output is enabled. The receiver 4 output goes into three-state, and the input presents a 30k load to ground.

When DCE/$\overline{DTE}$ is high, the driver 1 output goes into three-state, and the receiver 4 output is enabled. The receiver 4 input presents a 30k load to ground in all modes except when configured for RS232 operation, when the input impedance is 5k to ground.

Multiprotocol Interface with DB-25 or µDB-26 Connectors

A multiprotocol serial interface with a standard DB-25 connector EIA-530 pin configuration is shown in Figure 16. [Figures 16–19 follow on pp. 21–24]. The signal lines must be reversed

in the cable when switching between DTE and DCE using the same connector. For example, in DTE mode, the RXD signal is routed to receiver 3, but in DCE mode, the TXD signal is routed to receiver 3. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode-select pins. The single-ended driver 1 and receiver 4 of the control chip share the RL signal on connector pin 21. With $\overline{EC}$ low and CTRL/$\overline{CLK}$ high, the DCE/$\overline{DTE}$ pin becomes an enable signal.

Single-ended receiver 4 can be connected to pin 22 to implement the RI (ring indicate) signal in RS232 mode (see Figure 17). In all other modes, pin 22 carries the DSR(B) signal.

A cable selectable multiprotocol interface is shown in Figure 18. Control signals LL, RL and TM are not implemented. The V_{CC} supply and select lines M0 and M1 are brought out to the connector. The mode is selected in the cable by wiring M0 (connector pin 18) and M1 (connector pin 21) and DCE/$\overline{DTE}$ (connector pin 25) to ground (connector pin 7) or letting them float. If M0, M1 or DCE/$\overline{DTE}$ are floating, pull-up resistors R3, R4 and R5 will pull the signals to V_{CC}. The select bit M1 is hard wired to V_{CC}. When the cable is pulled out, the interface goes into the no-cable mode.

A cable-selectable multiprotocol interface found in many popular data routers is shown in Figure 19. The entire interface, including the LL signal, can be implemented using the tiny µDB-26 connector.

Conclusion

The LTC1343 and LTC1344 allow the designer of a multiprotocol serial interface to spend all of his time on the software rather than the hardware. Simply drop the chips down on the board, hook them up to the connector and a serial controller, apply the 5V supply voltage and you're off and running. In addition, the chip set's small size and unique termination topology allow many ports to be placed on a board using inexpensive connectors and cables. *LT*
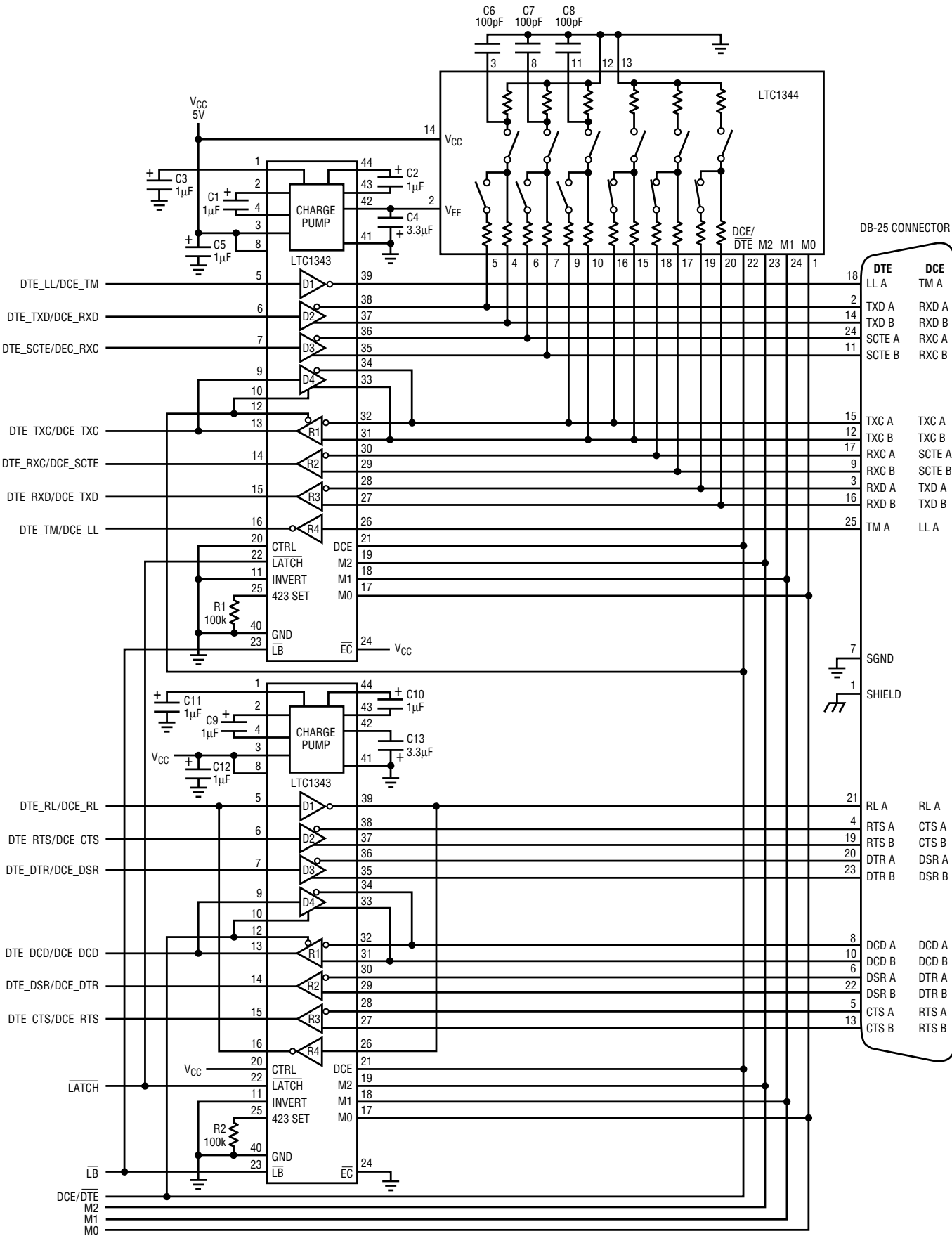
Figure 16. Controller-selectable multiprotocol DTE/DCE port with DB-25 connector
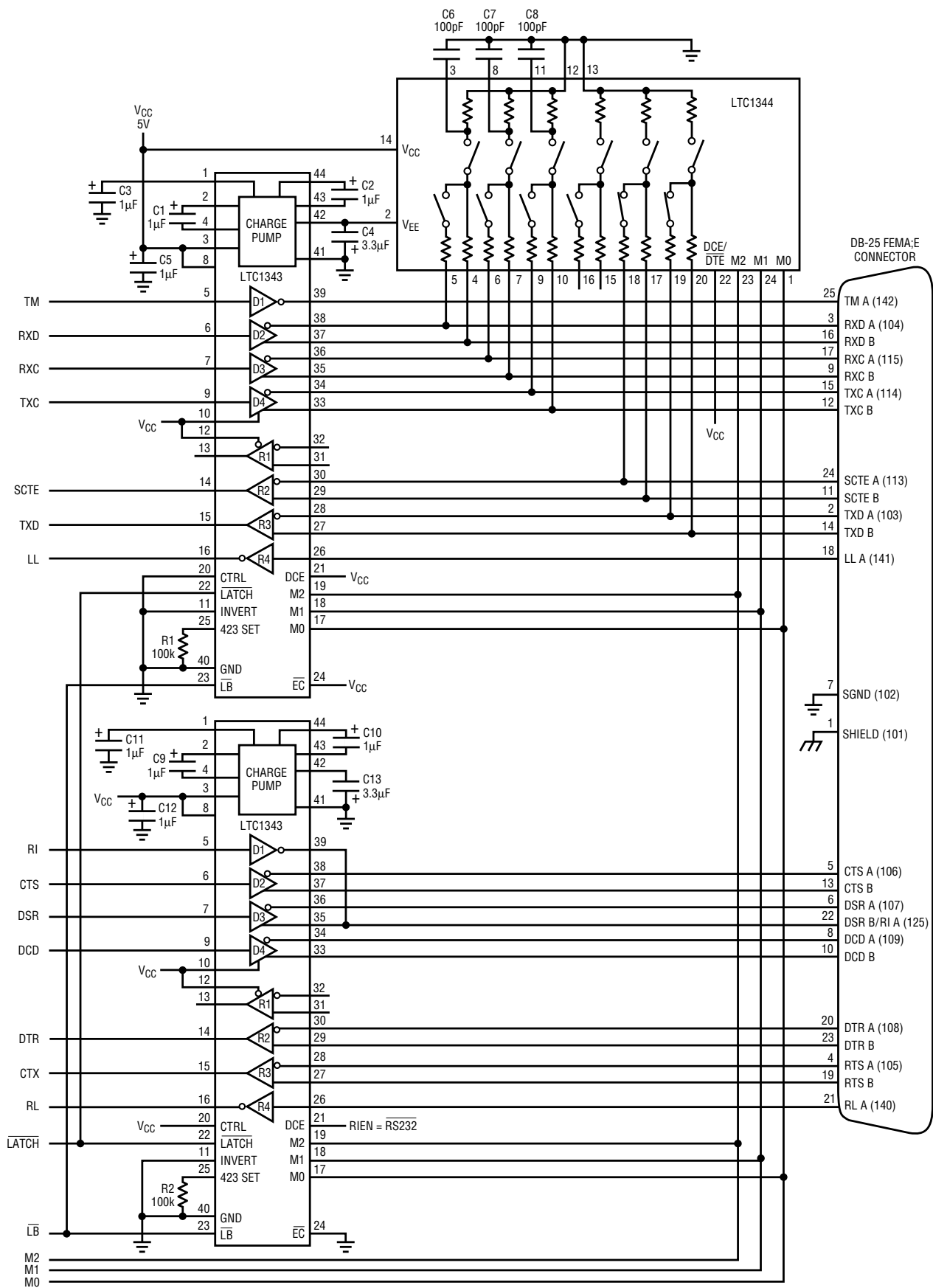
Figure 17. Controller-selectable multiprotocol DCE port with ring-indicate and DB-25 connector
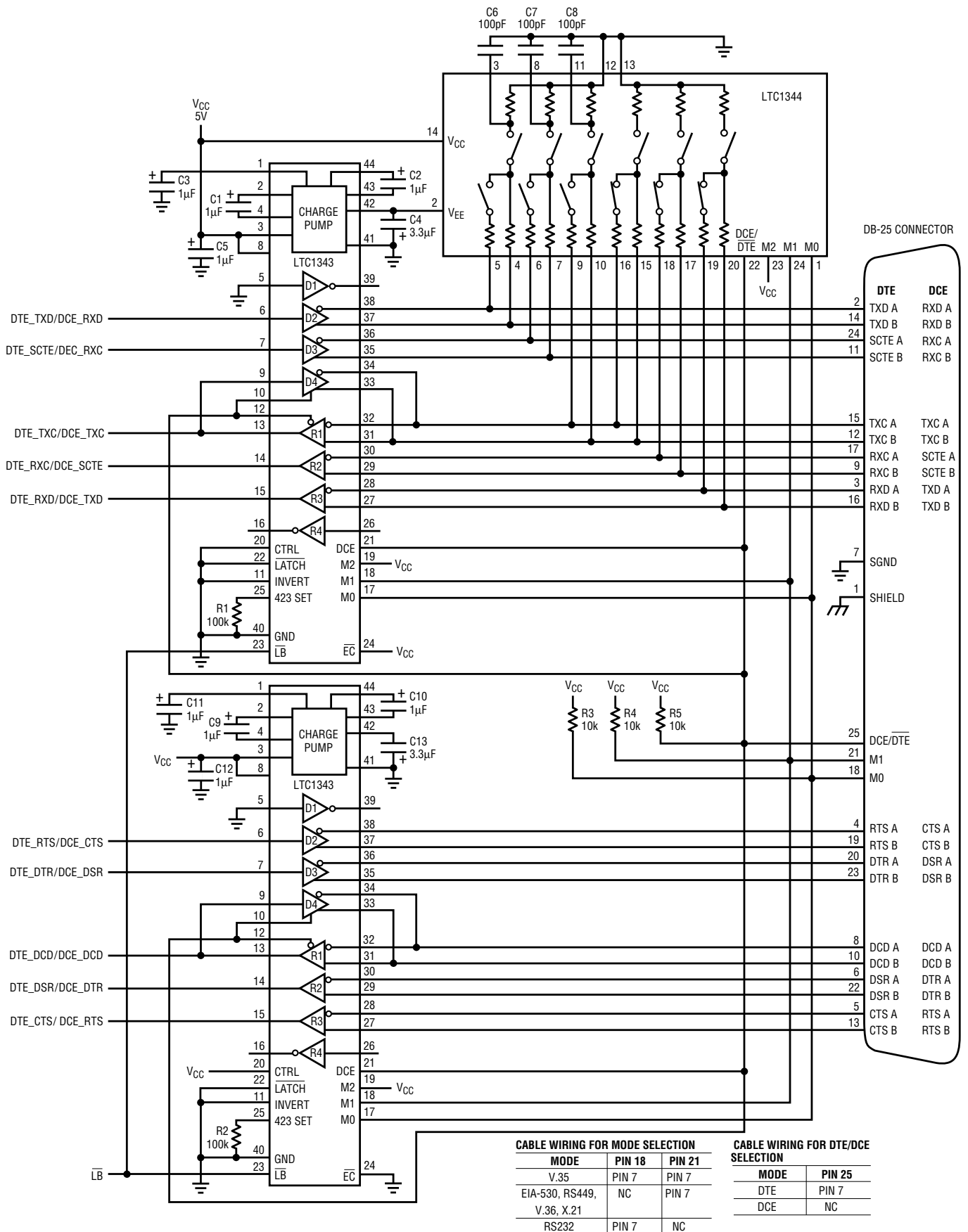
Figure 18. Cable-selectable multiprotocol DTE/DCE port with DB-25 connector

CABLE WIRING FOR MODE SELECTION		
MODE	**PIN 18**	**PIN 21**
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION	
MODE	**PIN 25**
DTE	PIN 7
DCE	NC

C6 100pF C7 100pF C8 100pF

LTC1344

μDB-26 CONNECTOR

V_CC 5V

CHARGE PUMP

LTC1343

V_CC
V_EE

C3 1μF C1 1μF C2 1μF C4 3.3μF C5 1μF

DTE_TXD/DCE_RXD
DTE_SCTE/DEC_RXC
DTE_TXC/DCE_TXC
DTE_RXC/DCE_SCTE
DTE_RXD/DCE_TXD

CTRL
LATCH
INVERT
423 SET
R1 100k
GND
LB
EC

DCE/DTE M2 M1 M0

V_CC

	DTE	DCE
2	TXD A	RXD A
14	TXD B	RXD B
24	SCTE A	RXC A
11	SCTE B	RXC B
15	TXC A	TXC A
12	TXC B	TXC B
17	RXC A	SCTE A
9	RXC B	SCTE B
3	RXD A	TXD A
16	RXD B	TXD B
7	SGND	
1	SHIELD	

CHARGE PUMP

LTC1343

C11 1μF C9 1μF C10 1μF C13 3.3μF C12 1μF

V_CC R3 10k V_CC R4 10k V_CC R5 10k

DTE_LL/DCE_LL
DTE_RTS/DCE_CTS
DTE_DTR/DCE_DSR
DTE_DCD/DCE_DCD
DTE_DSR/DCE_DTR
DTE_CTS/DCE_RTS

CTRL
LATCH
INVERT
423 SET
R2 100k
GND
LB
EC
LB

DCE
M2
M1
M0

	DTE	DCE
25	DCE/DTE	
21	M1	
18	M0	
4	RTS A	CTS A
19	RTS B	CTS B
20	DTR A	DSR A
23	DTR B	DSR B
8	DCD A	DCD A
10	DCD B	DCD B
6	DSR A	DTR A
22	DSR B	DTR B
5	CTS A	RTS A
13	CTS B	RTS B
26	LL B	LL B

CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION

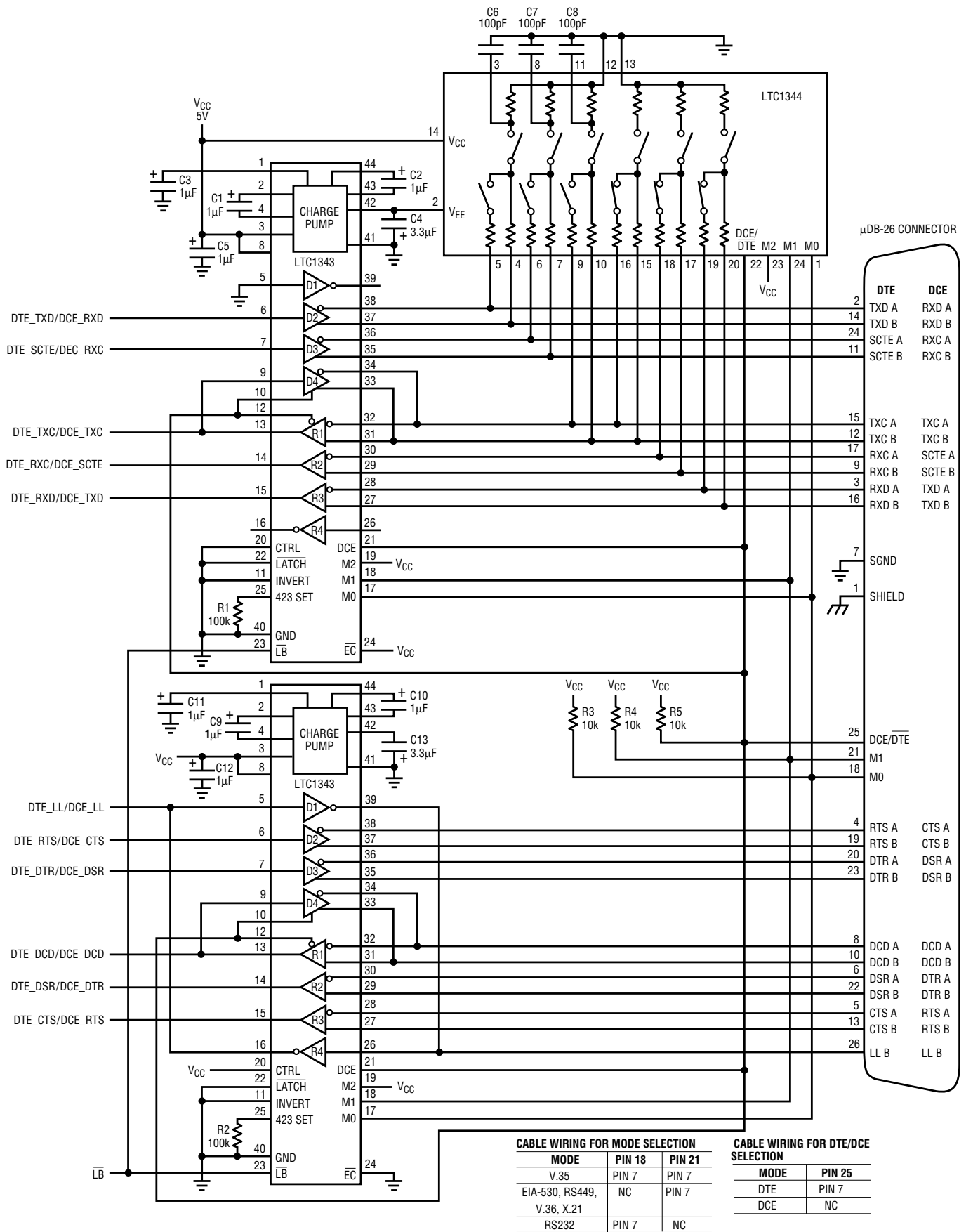| MODE	PIN 25
DTE	PIN 7
DCE	NC

Figure 19. Cable-selectable multiprotocol DTE/DCE port with μDB-26 connector

Li-Ion Battery Charger Does Not Require Precision Resistors

<div align="right">

by Arie Ravid

</div>

In constant-voltage mode charging, a Li-Ion cell requires 4.1V ±50mV. This 1.2% tolerance is tight. In a regulation loop where a voltage divider is compared against a reference, the accuracy is achieved by selecting a 0.7% reference and a voltage divider with 0.25% tolerance resistors. Unfortunately, 0.25% precision resistors cost three times as much as 1% resistors and have very long lead times.

One solution for moderate volume production involves adding two 1% resistors and two jumpers to the charger circuit, as shown in Figure 1. The jumpers are removed as necessary to bring the constant voltage to the required accuracy of 1.2%.

The charger selected for this example is the LT1510 and the number of Li-Ion cells in the battery is three. Select a value for R4 (20k) and calculate the values for resistors R1, R2 and R3 using the equations in Figure 1. K is the relative change required for a circuit with all its tolerances in one direction. For example, in the case of a 0.5% reference and

two 1% resistors, the total tolerance is 2.5%. In order to bring it back to 1.2%, the percentage change required is 2.5% – 1.2% = 1.3% and K = 0.013.

The jumpers J1 or J2 need to be opened based on the following:

If V_{OUT} is K/2 below nominal, remove J1.

If V_{OUT} is K/2 above nominal, remove J2.

The following values were calculated: R1 = 20k, R2 = 324Ω, R3 = 80.6Ω and R4 = 4.99k.

The voltage below which J1 should be opened is 12.34V – 1.3%/2 = 12.22V.

The voltage above which J2 should be opened is 12.34V + 1.3%/2 = 12.42V.

The complete schematic can be seen in Figure 2. Q3 is off when the charger is not powered, preventing current drain from the battery through the voltage divider. R5, a 100k resistor, isolates the OVP pin from any high frequency noise on V_{IN}. The charger in Figure 2 is programmed for 1.3A constant current. ∠⊤
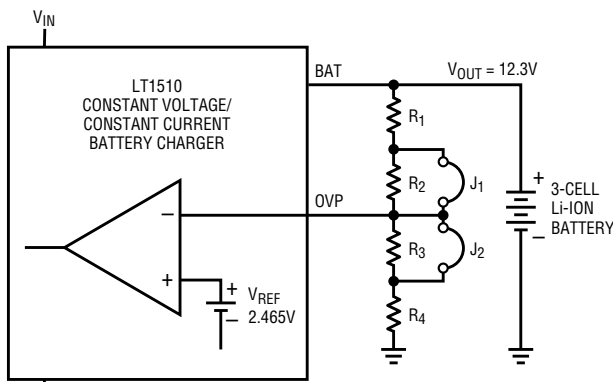
$$R1 = R4 \times \frac{V_{OUT} - V_{REF}}{V_{REF}}$$

$$R2 = (R1+R2) \times K$$

$$R3 = \frac{R4 \times K}{1 - (1 - K)\frac{V_{REF}}{V_{OUT}}}$$

Figure 1. R2, R3, J1 and J2 eliminate the need for precision resistors.

*TOKIN OR MARCON CERAMIC SURFACE MOUNT
** COILTRONICS CTX33-2

Figure 2. 3-cell Li-Ion charger without precision resistors

Constant-Voltage Load Box for Battery Simulation

by Jon Dutra

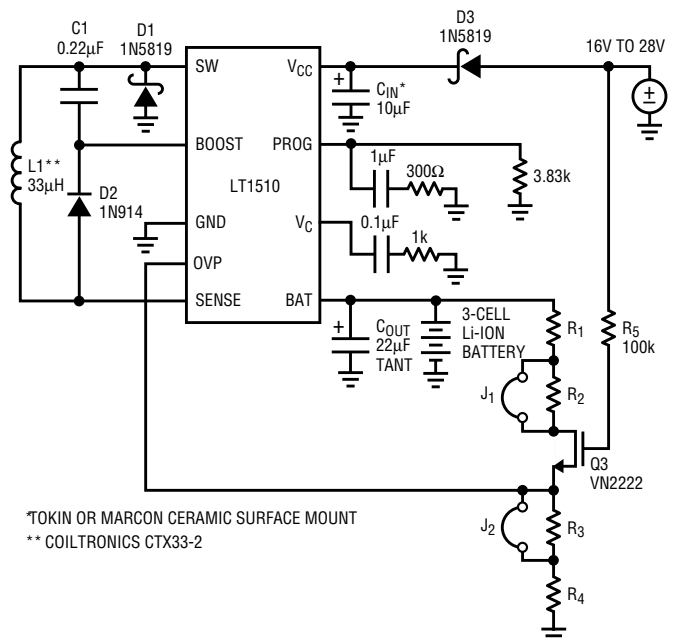Linear Technology has developed many new switcher-based battery charger ICs. Testing accuracy, regulation and efficiency in the lab with a battery load is inconvenient because the terminal voltage of a battery constantly changes as it is being charged. If much testing is to be done, a large supply of dead batteries will be needed, since one set of cells can quickly become overcharged. This Design Idea describes an active load circuit that can be used to simulate a battery in any state of charge. The battery simulator provides a constant-voltage load for a battery-charging circuit, independent of applied charging current. The simulator's impedance is less than 500mΩ at all reasonable input frequencies. Best of all, the simulator can never be overcharged, allowing long-term testing and debugging of a charger system without the possibility of battery damage.

Circuit Operation

The simulator uses an LT1211 high speed, single-supply op amp to drive the base of a high gain PNP transistor-stage active load. Power for the LT1211—a portion of the charging current—is supplied through a diode so the op amp and reference can survive brief periods of zero charging current. The op amp is configured for a DC gain of four, so the voltage on its noninverting input is one fourth of the voltage that the load box is set to. With S1 open, the load-voltage adjust range will be from 10V to 20V, and with S1 closed it will be approximately 3.5V–10V. Low voltage operation could be improved by replacing the top LT1004-2.5 with an LT1004-1.2 and reducing R1, the reference bias resistor, to 1k. The 510Ω and 1.1k resistors are required for high frequency stability; they suppress a

1MHz oscillation. The 1N5400 diode and 4-amp fuse protect the circuit from reverse voltages.

Results

The battery simulator circuit has been tested "swallowing" currents from 30mA to 3A with the output voltage essentially unchanged. When simulating a battery, the voltage adjust can be increased until the charger thinks the battery is fully charged and reduces the current into the simulator. Conversely, as the voltage is adjusted down, the battery charger may think the battery is becoming discharged and increase the current into the simulator.

Figure 2 shows the circuit's capacity for current absorption at two voltages, 5V and 15V, from 50mA to 3 amps. *LT*
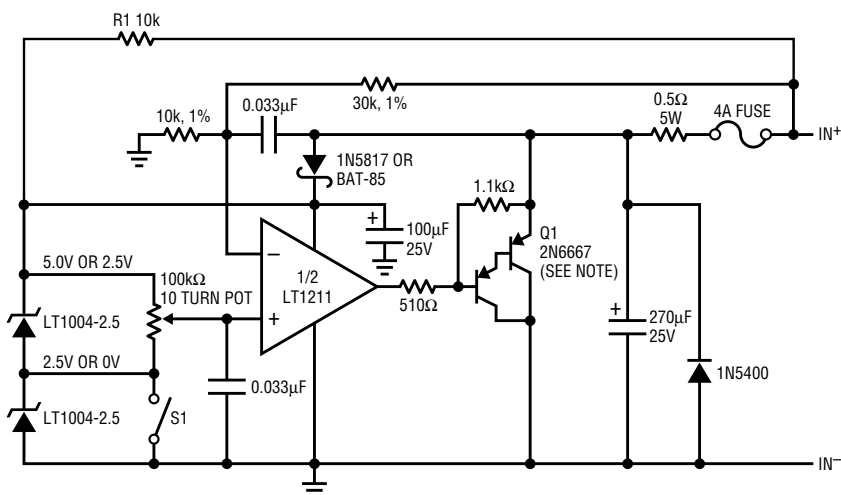
S1 CLOSED ≥ 0 TO 10V RANGE
S1 OPEN ≥ 10V TO 20V RANGE
ALL RESISTORS 5% UNLESS NOTED
Q1 DISSIPATES MOST OF THE POWER, MOUNT ON AN ADEQUATE HEAT SINK!

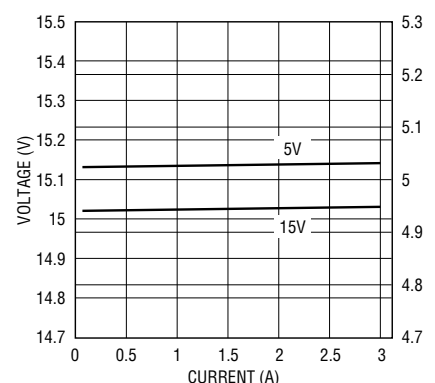**Figure 1. Schematic diagram of battery simulator**

Figure 2. Current absorption capacity of the battery simulator at 5V and 15V

LT1510 Charger with −ΔV Termination

by Arie Ravid

Any portable equipment that requires fast charge needs proper charge termination. Commonly, a LT1510 constant-voltage, constant-current type charger controlled by a microcontroller is used. Sometimes, however, a microcontroller is not available or is not suitable for fast-charge termination.

When fast charging NiCd batteries with constant current, the internal battery temperature rises toward the end of the charge. Since the temperature coefficient of NiCd is negative, the temperature rise causes the battery voltage to drop. The drop can be detected and used for termination (called −ΔV termination). The circuit in Figure 1 is a solution for a 3-cell (Panasonic P140-SCR) NiCd battery charger with −ΔV termination.

U1 in Figure 1 is programmed by resistor R2 for a conservative charge current of 0.8A, which is 0.57**C**. Typi-

cal fast-charge current is 1**C**. (The boldfaced **C** represents a normalization concept used in the battery industry. A **C** rate of 1 is equal to the capacity of the cell in ampere-hours, divided by 1 hour. Since the capacity of the P140-SCR is 1.4 ampere-hours, **C** is 1.4 amperes.)

To determine the voltage droop rate, the battery was connected to an LT1510 charger circuit programmed for a 0.8A constant-current. The data was plotted as voltage versus time and the results are shown in Figure 2. The voltage slope is calculated to be −0.6mV/s. After the battery voltage dropped 300mV from the peak of 4.93V (100mV per cell), the charger was disabled.

At the heart of the circuit in Figure 1 is U3, a sample-and-hold IC (LF398). For every clock pulse at pin 8, the output of U3 (pin 5) updates to the input level on pin 3. When the battery

voltage drops, the input to U3 also drops. If the update step at the output of U3 is sufficiently negative, U2B latches in the high state and Q1 turns on. Q1 terminates the charge by pulling down the LT1510's V_C pin, and thereby disabling it.

U2A and the associated passive components smooth, amplify and level shift the battery voltage. The timer (U4) updates the hold capacitor (C8) every fifteen seconds. The timer signal stays high for 7ms, sufficient time for the hold capacitor to be charged to the input level. U2B and the associated parts form a latch that requires a momentary negative voltage at pin 6 to change state. R15 supplies the negative feedback and Q2, R16, R17 and C10 reset the latch on turn-on.

U3's output voltage droops at a rate proportional to the hold capacitor's internal leakage and the
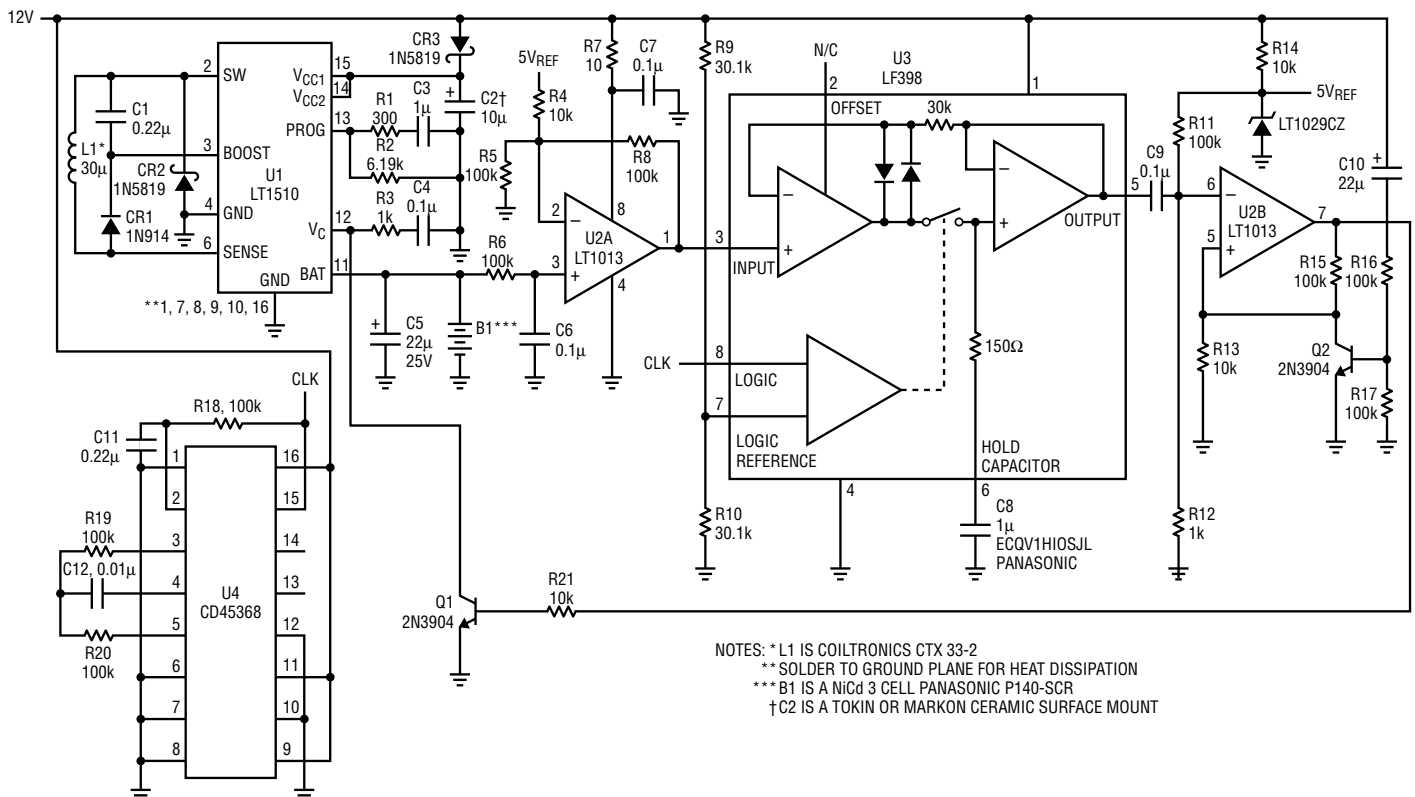
Figure 1. Schematic diagram: 3-cell NiCd charger with −ΔV termination

Transparent Class-D Amplifiers Featuring the LT1336

by Dale Eagar

Introduction

Efficiency in the field of power conversion is like transparency in the field of light transmission. It is no wonder, then, that Class-D amplifiers are often called transparent, since they have no significant power losses. In contrast to class-D amplifiers' nearly lossless switching, class-A through class-C amplifiers are throttling devices that waste significant energy. Amplifiers of the "lower classes" (A–C) are modeled as rheostats (variable resistors), whereas class-D amplifiers are modeled as variacs (variable transformers). The ideal resistor dissipates power, whereas the ideal transformer does not. Like transformers (variacs), many class-D amplifiers can transfer energy in both directions—input to output and output to input.

Class-D amplifiers also have a way of ignoring reactive loads that can be uncanny. A class-D amplifier operating with an AC output will draw very little additional input power when a sizable capacitive or inductive load is placed at its output. This is because the reactive load has AC voltage across it and AC current flowing through it, but the phase angle of the voltage and current is such that no real power is dissipated. The class-D amplifier ends up shuttling power back and forth between its input and its output, doing both with minimal loss. An ideal class-D amplifier can be thought of as having no place to dissipate power, since all of its components are lossless; that is, it contains no resistors.

The Electric Heater— a Simple Class-D Amplifier

Class-D amplifiers can be simple or complex, depending on what is required by the application. A simple class-D amplifier is the thermostatic switch in an electric heater. The thermostat controls the heater by turning it on or off. The switch is essentially lossless, dissipating practically no power. This class-D amplifier is remarkably efficient, since even the energy lost in the switch, power cord and house wiring contributes to the desired result. The duty factor, and hence the average amount of power delivered to the heater, can assume an infinite number of values. This is true even though a constant amount of heat is delivered when the heater is on.
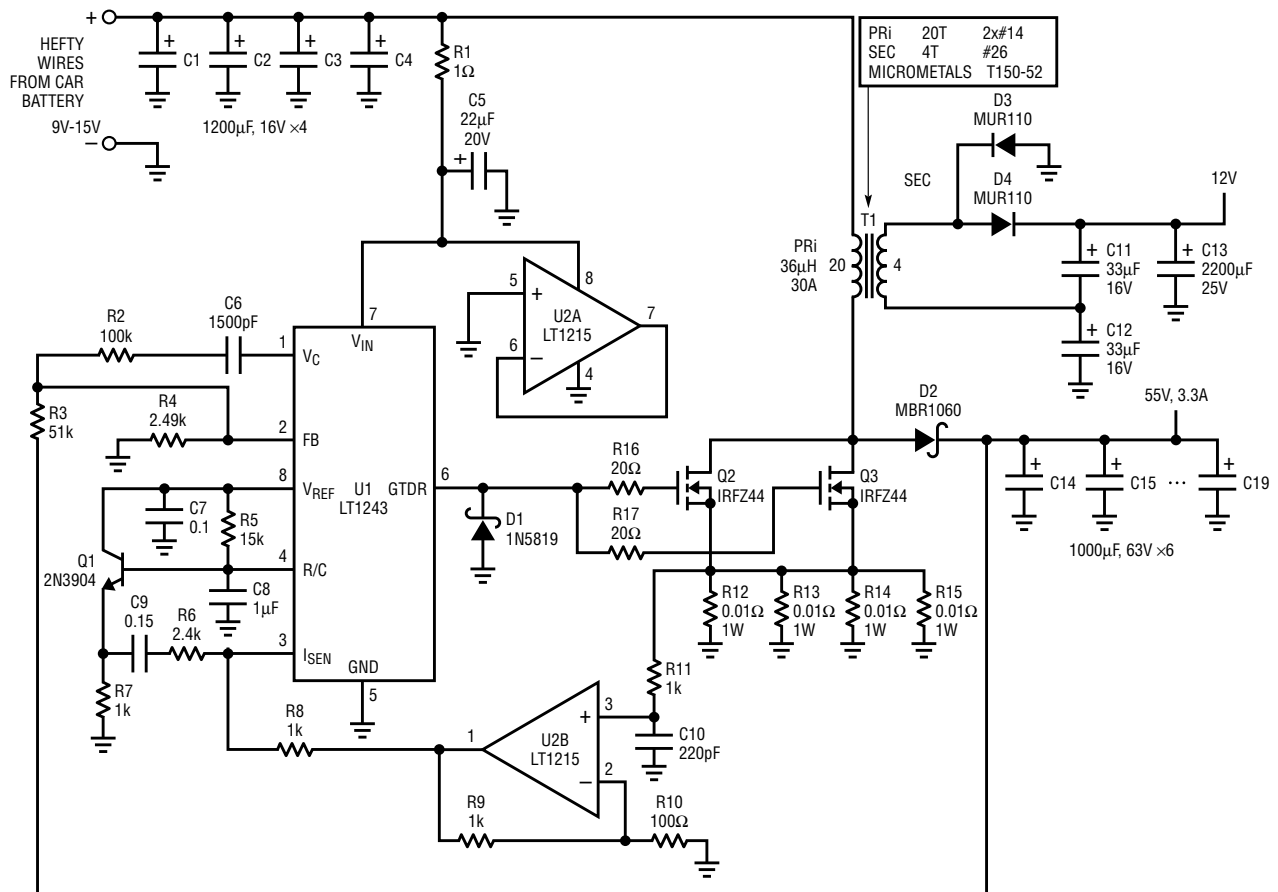

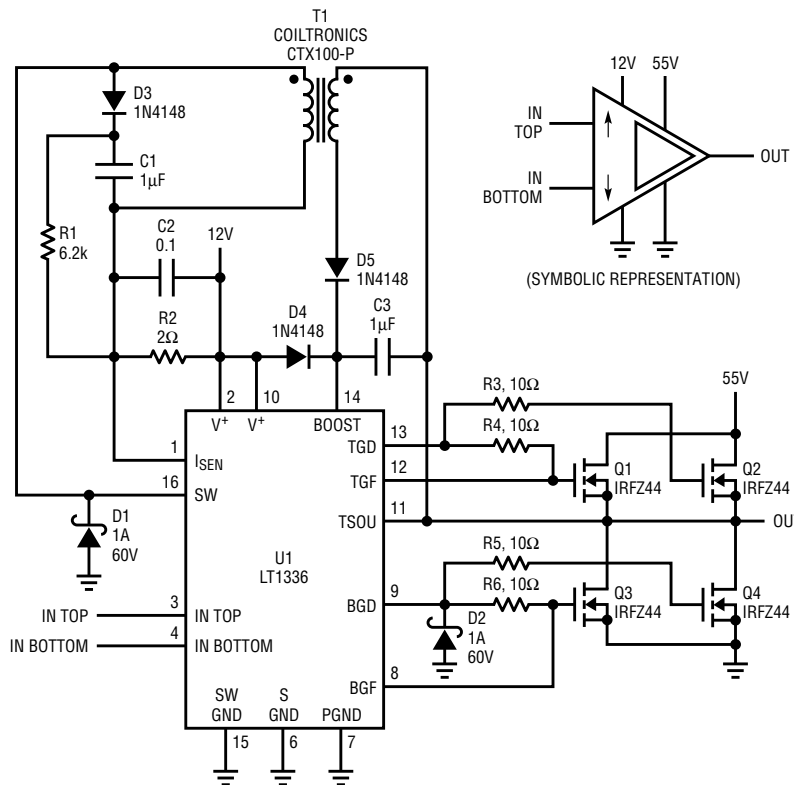Figure 1. 200W, 12V to 60V front end for automotive applications

Figure 2. Half-bridge driver subcircuit and symbolic representation

Quadrants of Energy Transfer

Class-D amplifiers have a property that requires new terminology, a property that generally isn't considered in lower-class amplifiers. This property, quadrants of energy transfer, describes the output characteristics of the class-D amplifier. The output characteristics are plotted on a imaginary X-Y plot (I've yet to see someone actually do one on paper), one axis representing output voltage and the other axis representing output current, with the intersection of the axes representing zero volts and zero amps. A simple switcher that can only provide a positive output current into a positive output voltage can be described as a 1-quadrant device. This 1-quadrant device could be a computer power supply, a battery charger or any supply that delivers a positive voltage into a device that can only consume power.

The 2-quadrant converter can be one of two different things: 1) A positive output voltage that can both source and sink current, or 2) A posi-

tive current that can comply both positive and negative output voltage. Finally, the 4-quadrant converter can both source and sink current into both positive and negitive output voltages.

1-Quadrant Class-D Converter

To illustrate the 1-quadrant class-D amplifier, we will focus on the boost mode converter detailed in Figure 1 This circuit removes power from the source (12V automotive battery) and delivers it to the load (some as-yet-unknown 55V device) This circuit is classified as "1 quadrant" because it can only regulate output voltage in one polarity (positive) and it can output current in only one polarity (positive).

Introducing the LT1336 Half-bridge Driver

Taking a side step from our main discussion, we will introduce a component, the half-bridge power am-

plifier. Figure 2 details the LT1336 driving power MOSFETs and shows the symbolic representation of this subcircuit that will appear in subsequent figures. Table 1 shows the logical states of this half-bridge power driver.

4-Quadrant Class-D Amplifier

Class-D amplifiers are commonly used in subwoofer drivers. This is because subwoofers require a great deal of power. A class AB amplifier driving a subwoofer will put about half of its input power into its heat sink. Driving the same subwoofer at the same volume with the same music, a class-D amplifier will put about five percent of its input power into the heat sink. The difference is ten to one on the heatsink size and two to one on the input power supply. Figure 3 is the 200W class-D subwoofer driver. This circuit uses the 200W front end developed in Figure 1 as its power source. The circuit in Figure 3 performs as follows: U1a, R1–R4 and C7 implement a 75kHz pseudosawtooth oscillator. U1d is the input amplifier/filter, with a gain of 6.1 and 200Hz Butterworth lowpass response. U1b and U1c are comparators that compare the sawtooth and the amplified/filtered input signal to form two complimentary, pulse-width modulated square waves. X1 and X2 are two half-bridge power drivers and M1 is the subwoofer driver.

One of the properties of Class-D, 4-quadrant amplification is the ability to transfer power both to and from the load. In our subwoofer driver, this happens when the driver reaches the end of any given excur-

Table 1. Half-bridge power driver truth table

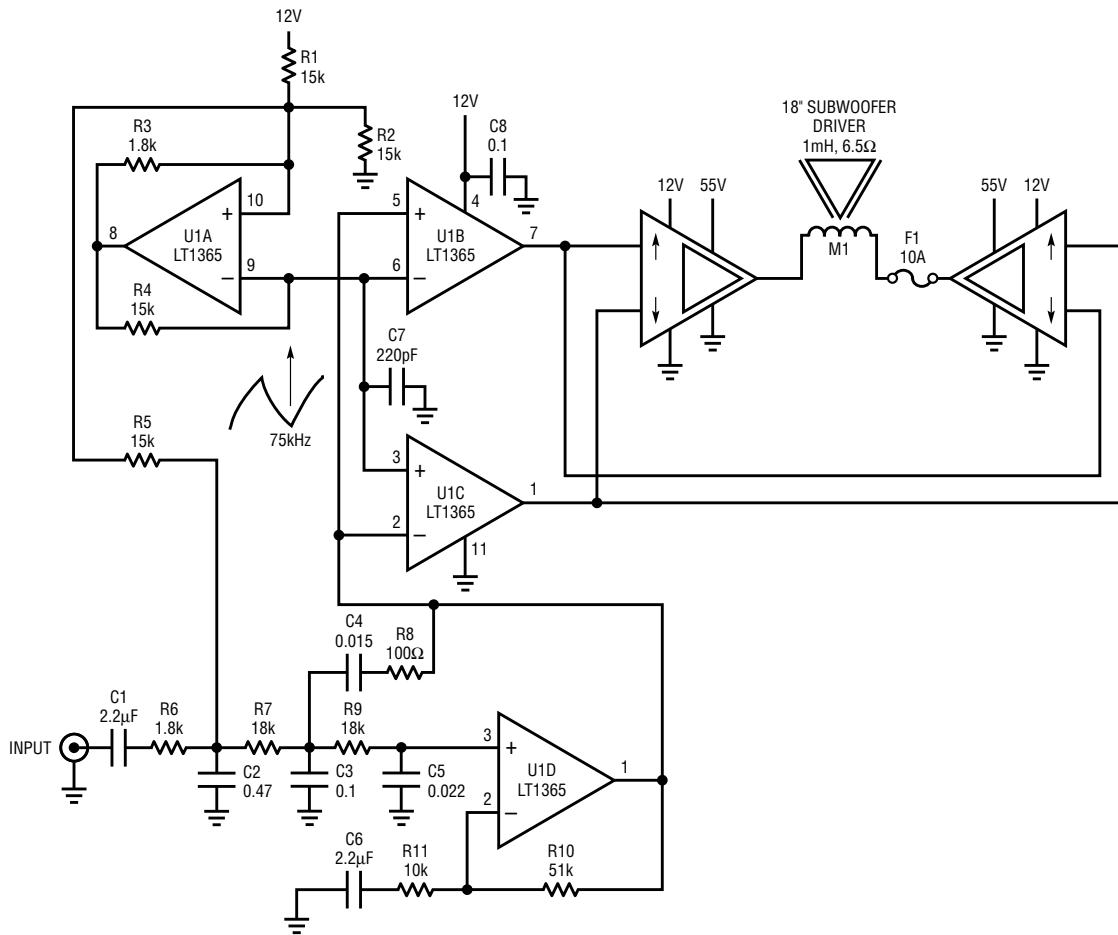| In Top	In Bottom	Output
L	L	Floating
L	H	Ground
H	L	55V
H	H	Floating

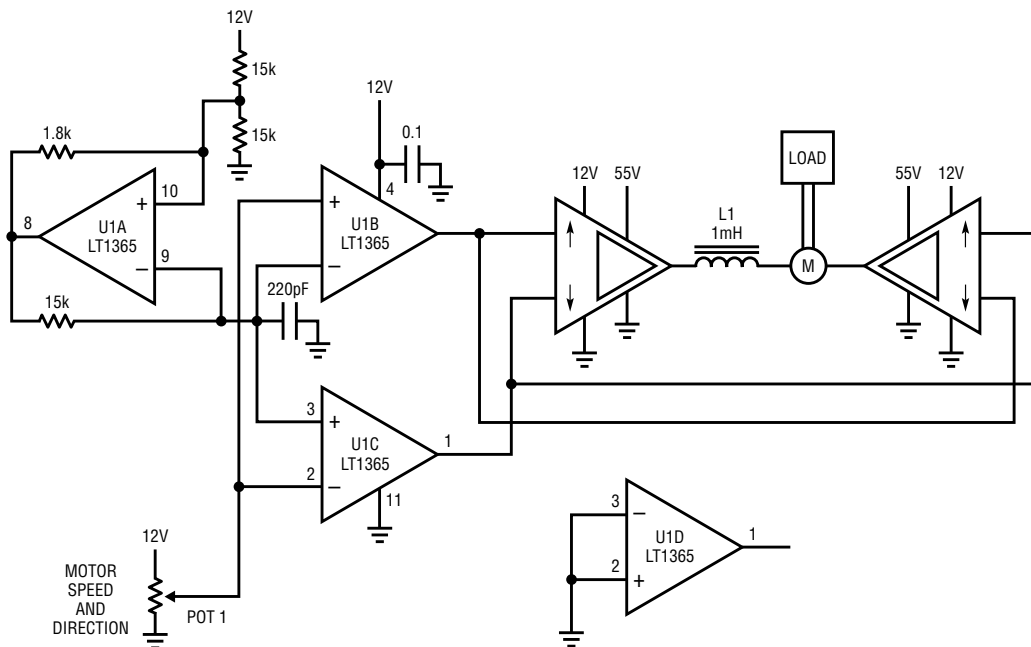**Figure 3. 200W-powered subwoofer**
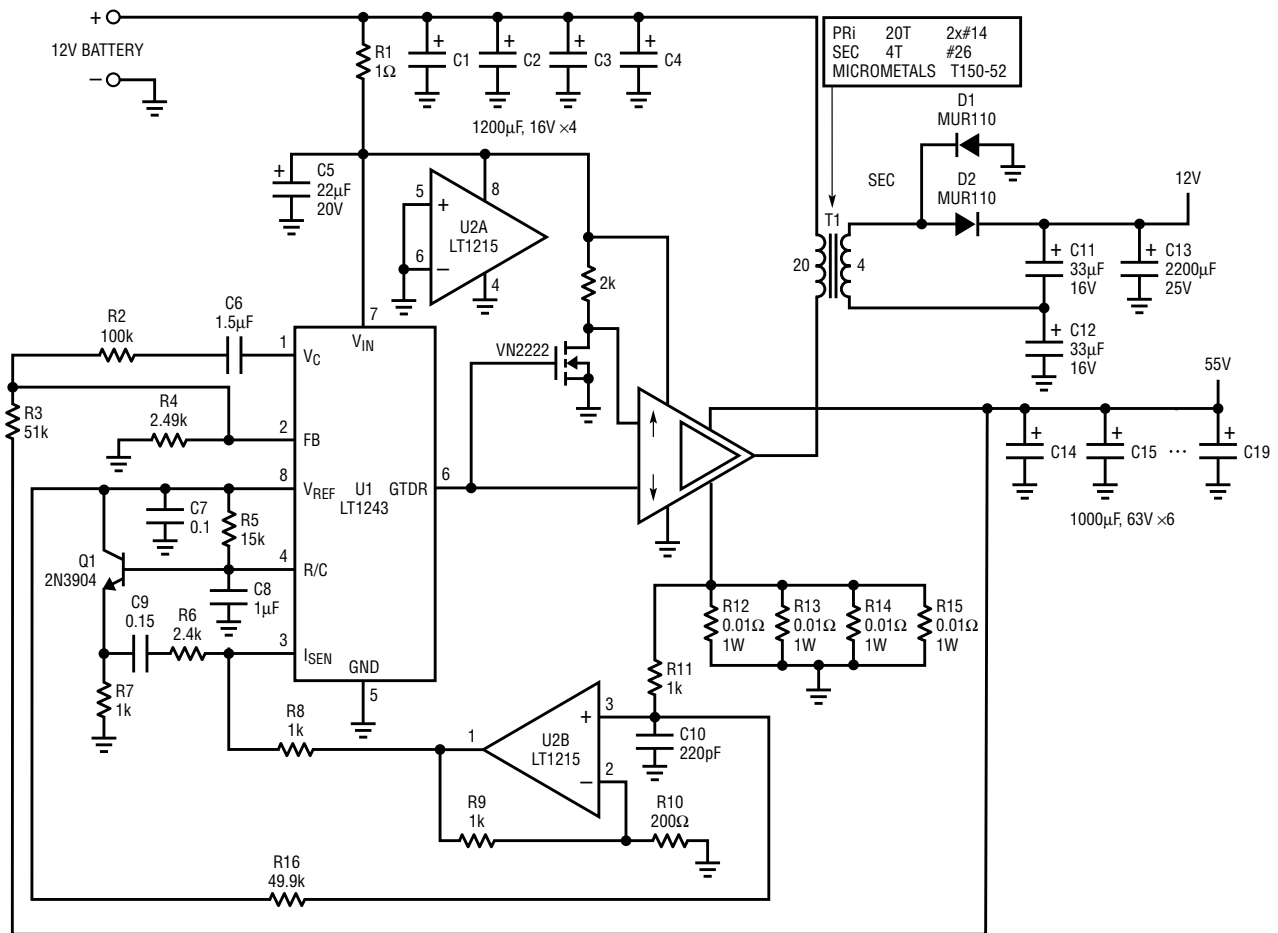
Figure 4. Class-D motor drive

Figure 5. 200W, 2-quadrant front end for automotive applications

sion and the combination of the driver spring and the acoustic spring drive the cone back to center. During this time, energy is transferred from the driver back to the input of the class-D amplifier stage. In the case shown in Figure 3, the energy ends up on the 55V bus, where the bus voltage climbs during these periods of "negative energy delivered to the load." Fortunately, C14–C19 of Figure 1 can store this energy; otherwise the 55V bus would subject to excessive voltage until someplace was found for the energy to go.

Class-D for Motor Drives

Substituting a motor and an inductor for the subwoofer in Figure 3 and simplifying the control, we arrive at the circuit shown in Figure 4. Connecting this circuit to the front end shown in Figure 1 and then getting the motor up to speed is no problem,

but when one wants to slow the motor down by turning pot 1 back toward its center, disaster strikes. Rotational energy stored in the inertia of the motor is converted back into electrical energy by the motor and is presented to the output of the class-D amplifier. L1, X1 and X2 do their job by transferring the energy back into the 55V bus. The energy goes into C14–C19 of Figure 1, charging them to some voltage significantly above 55V, and something breaks. The problem here is that the circuit in Figure 1 is only a 1-quadrant class-D amplifier.

Managing the Negative Energy Flow

Sound like a course in management? The negative energy transferred through the class-D amplifier needs a home. One simple home is the 62V power Zener diode strapped across the 55V bus and bolted to a massive

heat sink. One could easily imagine the heat sink as the brake shoes heating up as the electric vehicle winds down the mountain road. Another place to put the energy is back into the 12V battery. This will require upgrading the 12V to 55V front-end power converter from 1 quadrant to 2 quadrants.

The 2-Quadrant Class-D Converter

Converting Figure 1 to two quadrants involves replacing D2 with a switch and activating the switch out of phase with the switch formed by Q2 and Q3. The half-bridge power driver shown in Figure 2 is just such a switch. Refer to Figure 5. The I_{SENSE} signal (U1, pin 3) needs to be offset to accommodate negative current (add R16, Figure 5) The I_{SENSE} signal needs to be scaled for twice the range (–30A to 30A rather

than 0A to 30A); this is done by changing R10.

Now we are happily winding down the mountain road, watching the scenery unfold before us. We are happy in knowing that we are recycling the energy released from the descent by charging our batteries, while watching the mountain bikers burn their descent energy off in brake linings. Once again technology wins over sweat and brawn.

A Trip Over the Great Divide

Climbing the great divide in an electric vehicle requires some planning. Stops to recharge are necessary. Once on top, the whole scheme changes: descending the hill, charging our battery, all goes well until the battery is fully charged; then we have to stop. Further descent would overcharge our battery, boiling out the electrolyte. Not only would this ruin our battery,

in the end we would have no place to put the energy and our class-D amplifier would find some way to fail. We need to stop and drain off some charge, trade batteries with someone climbing the other side or put a power Zener on our battery. Figure 6 details the active Zener circuit. Using the reference in U1 of Figure 5 and the unused half of U2 we are able to make a hysteretic clamp that puts all of the heat into a resistor, R5. This circuit will save the battery from destruction and drop our level of smugness back to that of the mountain bikers.

Conclusion

Class-D has been around for a long time: the venerable electric heater with its bang-bang controller is a remarkably efficient and reliable class-D amplifier. Class-D drives have been used for decades in golf carts, fork lifts, cranes and industry. The advent of the half-bridge driver greatly simplifies the Class-D Amplifier. Here at Linear Technology we have a family of half/full bridge MOSFET drivers. For further information, contact us at the factory or refer to the LT1158, LT1160, LT1162 or LT1336 data sheets. *LT*
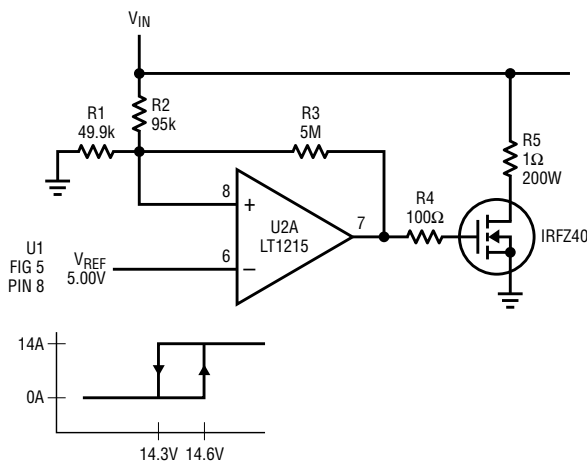

Figure 6. Wolf Creek Pass adapter

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leakage current at pin 6 (10pA typical). This droop is very low and does not affect the operation of the circuit.

The minimum negative battery voltage slope required to trigger termination (–dV/dT) is 0.3mV/s. It can be calculated from:

$$-dV/dT = V_{TRIG}/(T_{CLK} \times G_{U2A})$$
where:
V_{TRIG} is the trigger voltage of U2B,
$$V_{TRIG} = V_{REF} \times R12/(R11 + R12)$$
$$= 5 \times 1/101 = 49.5mV$$
$$V_{REF} = 5V$$
T_{CLK} is the clock period, 15 seconds,
G_{U2A} is the gain of the first stage,
$$= R8/(R4 \| R5)$$
$$= 11$$

The circuit in Figure 1 was built and connected to a system that discharges the battery to 3V after termination, at constant current of
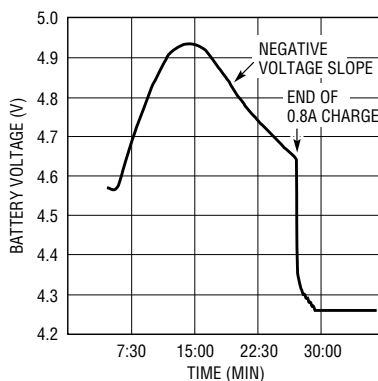
Figure 2. Voltage-droop rate, 3-cell NiCd battery

0.8A. Once the battery drops to 3V, the system reenables charging, and thus the complete system repeats charge/discharge cycles indefinitely. The duration of 70 charge discharge cycles was recorded. The following is condensed data from the test:

1. Average Charge Time: 2:00:55 Hours

2. Standard Deviation of Charge Time: 5:37 Minutes

3. Average Discharge Time: 1:59:14 Hours

4. Standard Deviation of Discharge Time: 48 Seconds.

The ratio of standard deviation of charge time to average charge time proves that the charger has good repeatability. However, the ratio of standard deviation of discharge time to average discharge time shows that the charge level at the time of termination is very consistent because the discharge time at constant current is a better measure of charge level than charge time. A secondary termination method, such as time, battery temperature, or the like, is also recommended. *LT*

An Ultralow Quiescent Current, 5V Boost Regulator

by Sam Nork

Many battery-powered applications require an auxiliary 5V supply to power infrequently used circuitry, such as smart card readers, wireless i.d. tags, or the like. Keeping the 5V supply permanently active is desirable, since this eliminates timing delays and inrush currents due to supply start-up. The downside is that most 5V boost converters consume an unacceptable amount of quiescent current under no-load conditions. This problem is addressed by the SHDN features of the LTC1516

micropower, charge-pump DC/DC converter. Toggling the SHDN pin of the LTC1516 allows the 5V supply to remain in regulation with a typical no-load input current of less than 5µA. When the 5V output load is enabled, the part can supply up to 50mA of load current.

The LTC1516 produces a regulated 5V output from a 2V to 5V input (refer to Figure 1). In normal operation, the part regulates by sensing the output through a resistive divider and enabling a switched-capacitor

charge pump when the output droops below the trip point of the sense comparator (COMP2). When the output has been boosted above COMP2's upper trip point, the charge pump is turned off. In shutdown mode, the output load is disconnected from V_{IN} and the quiescent current drops below 1µA.

When the output is in regulation, the internal sense resistor draws only 1.5µA (typical) from V_{OUT}. During no-load conditions, this internal load causes a droop rate of only 150mV per second on V_{OUT} with C_{OUT} = 10µF. Applying a 5Hz–100Hz, 95%–98% duty-cycle signal to the SHDN pin ensures that the circuit in Figure 2 comes out of shutdown frequently enough to maintain regulation during no-load (or low-load) conditions. Since the part is kept in shutdown mode for the majority of the time, the no-load quiescent current (see Figure 3) is approximately equal to (V_{OUT} × (1.5µA + I_{LOAD}))/(V_{IN} × efficiency).

The LTC1516 must be taken out of shutdown mode for a minimum of 200µs to allow the internal sense circuitry to start up and keep the output in regulation. As the V_{OUT} load current increases, the frequency with which the part is taken out of shutdown must also be increased to prevent V_{OUT} from drooping below 4.8V during the OFF phase (see Figure 4). A 100Hz, 98% duty cycle signal
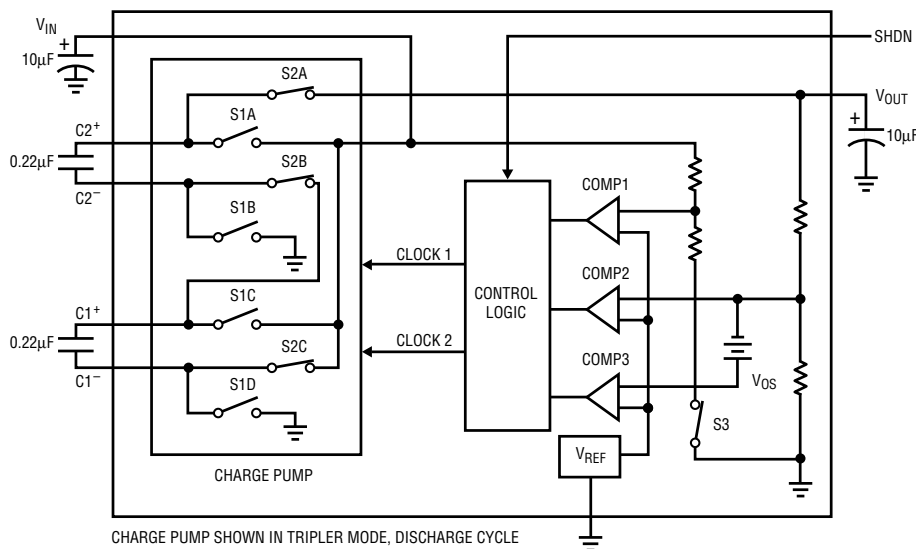
Figure 1. LTC1516 simplified block diagram
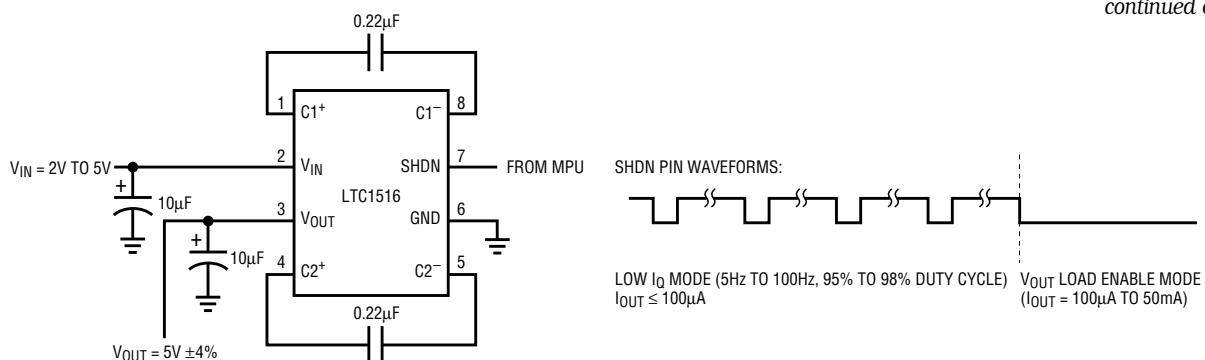

Figure 2. Ultralow quiescent current (<5µA) regulated supply

24 Volt to 14 Volt Converter Provides 15 Amps

by John Seago

The LTC1435 is an extremely versatile voltage controller. Most applications take advantage of its ease of design and the high efficiency of its synchronous regulator topology for microprocessor-level output voltages. The LTC1435 can also be used as a conventional buck regulator, with very high efficiency, in circuits requiring hundreds of watts and higher-than-logic-level output voltages. As a constant-frequency, current mode, step-down switching regulator, it controls external N-channel MOSFETs for very efficient, low noise operation. The current mode architecture provides a tightly controlled output voltage with excellent load and line regulation. Internal slope compensation eliminates subharmonic oscillations. The 1% reference ensures good initial set-point accuracy. The switching frequency can be set between 50kHz and 400kHz, so circuit efficiency, component size and transient response can be properly balanced. The LTC1435 also features both logic-level on/off control and output current soft-start. When the controller is turned off, voltage is removed from the load and quiescent input current drops to a mere 15µA. The LTC1435 is available in the popular 16-pin SO package.

Combining the LTC1435 with a large geometry power MOSFET and good PCB layout allows large currents to be processed easily and efficiently. With the use of a current sense transformer, output voltages greater than 10V can be implemented. The circuit in Figure 1 shows an LTC1435 configured as a conventional buck regulator using a single N-channel MOSFET to control an output voltage greater than 10V with load current exceeding 15 amps. The efficiency of the breadboard measured 94% with a 24V input, 14V output and 15A of load current. If maximum efficiency is required, adding a sec-
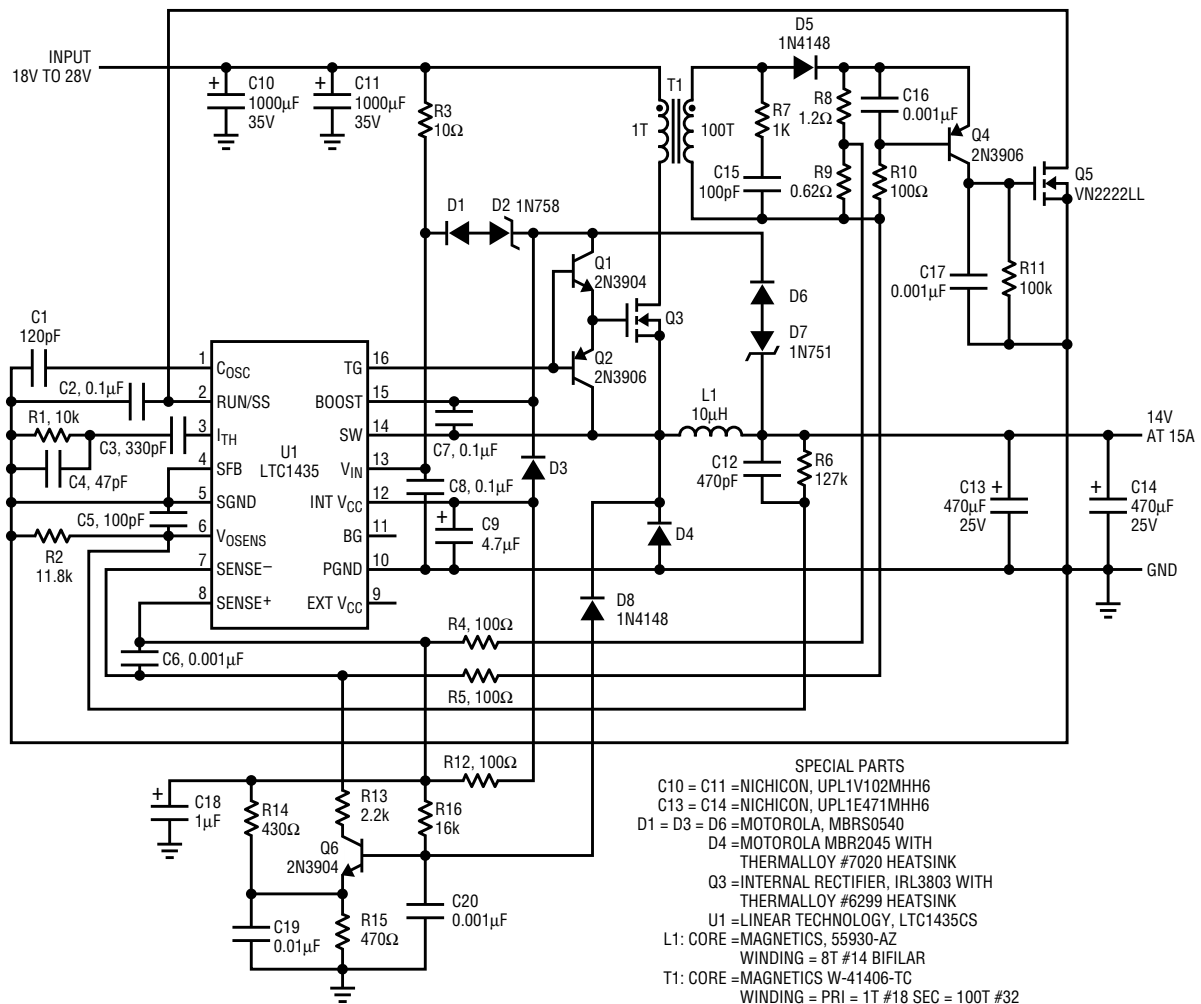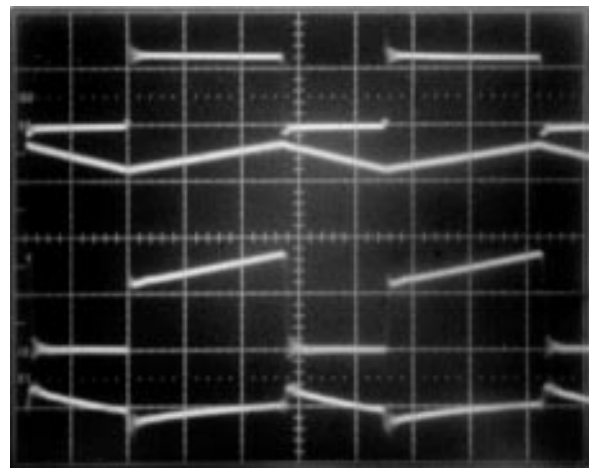

Figure 1. 14V, 15A buck regulator

ond power MOSFET for synchronous switching will improve efficiency by about 1%.

This circuit's 100kHz switching frequency was selected to reduce switching losses so that PCB mounted heat sinks could be used without requiring additional air flow. The switching frequency can be set from 50kHz to 400kHz by selecting an appropriate value for C1. The current sense transformer T1 uses a 1:100 turns ratio to scale down the buck inductor input current and develop the voltage across R9, used by the ±SENSE inputs for regulation. Short-circuit protection is provided by Q4 and Q5. When the current transformer secondary voltage developed across R8 and R9 is enough to turn on Q4, Q5 temporarily pulls the RUN/SS pin low, turning off the regulator. Output current soft-starts when Q5 releases the RUN/SS pin. This results in frequent attempts to establish output voltage if a short exists, without high current continuously flowing through the power elements. The power elements consist of input capacitors C10 and C11, Current sense transformer T1, buck inductor L1, power MOSFET Q3, commutating diode D4 and output capacitors C13 and C14.

Although the wide 3.6V–36V input voltage range and 99% duty cycle operation of the LTC1435 are ideal for

A = Q3 SWITCH VOLTAGE 20V/DIV
B = L1 CURRENT 10A/DIV
0.0V
0.0A
C = T1 PRIMARY CURRENT 10A/DIV
0.0A
D = OUTPUT VOLTAGE RIPPLE 0.2V/DIV   14VDC
2µs/DIV

Figure 2. Buck regulator circuit waveforms

battery/wall adapter input applications, operating above 95% duty cycle causes problems for the current sense transformer. To avoid transformer saturation, the Q6 stage limits duty cycle to approximately 90%. Current through R16 tries to charge C20 to the 3V base voltage of Q6. If the switch cycle terminates at less than a 90% duty cycle, C20 is reset by D8. If the duty cycle exceeds 90%, C20 charges until Q6 turns on, ending the switch cycle.

Switch voltage, inductor current, T1 primary current, and output voltage ripple waveforms are shown in Figure 2. These waveforms were measured with a 24V input, 14V output, and 15A load current. When MOS-

FET Q3 turns on, the switch voltage (Trace A) goes high, the inductor current (Trace B) increases, as does the T1 primary current (Trace C) and the output ripple voltage (Trace D). When Q3 turns off, the switch voltage goes low, inductor current decreases as its stored energy supplies load current through D4, T1 primary current goes to zero and the output voltage decreases slightly.

In addition to its role as a microprocessor voltage controller, the LTC1435 and current sense transformer can be very useful in higher voltage and higher current application where high efficiency and ease-of-design are important. *LT*

5V Boost Regulator, continued from page 33

on the SHDN pin ensures proper regulation with load currents as high as 100µA. When load current greater than 100µA is needed, the SHDN pin must be forced low, as in normal operation. The typical no-load supply current for this circuit with V_{IN} = 3V is only 3.2µA. *LT*
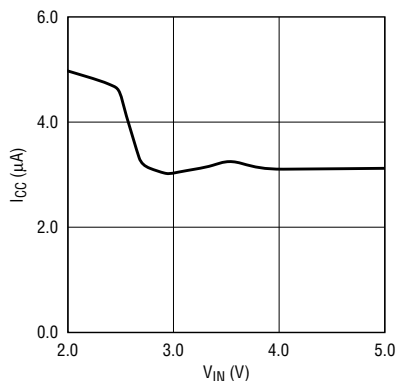
Figure 3. No-load I_{CC} versus input voltage for Figure 2's circuit

Authors can be contacted at (408) 432-1900

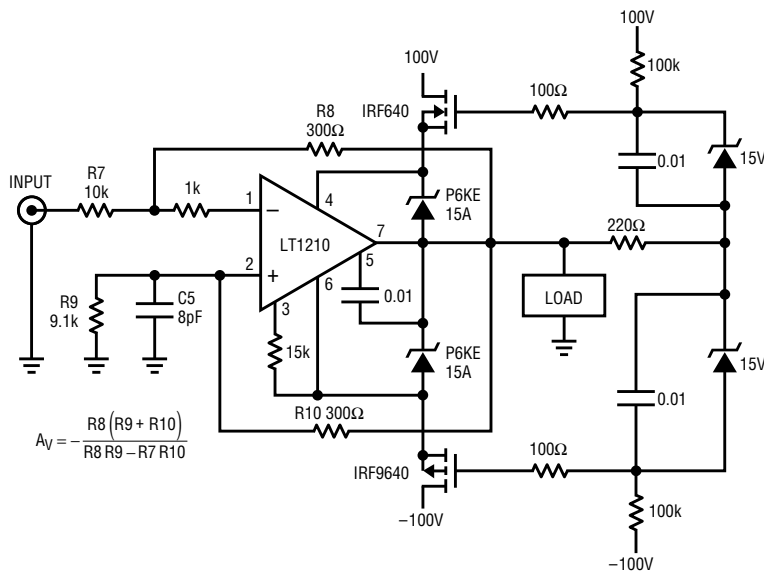**Figure 4. Maximum SHDN OFF time versus output load current for ultralow I_Q operation**

The LT1210: High Power Op Amp Yields Higher Voltage and Current

by Dale Eagar

Introduction

The LT1210, a 1 amp current feedback operational amplifier, opens up new frontiers. With 30MHz bandwidth, operation on ±15V supplies, thermal shutdown and 1 amp of output current, this amplifier single handedly tackles many tough applications. But can it handle output voltages higher than ±15V or currents greater than 1 ampere? This Design Idea features a collection of circuits that open the door to high voltage and high current for the LT1210.

Fast and Sassy— Telescoping Amplifiers

Need ±30V? Cascading LT1210's will get you there. This circuit (Figure 1) will provide the ±30V at ±1A and has 13MHz of full-power bandwidth (see Figure 2). How does it work? The first LT1210 drives the "ground" of the second LT1210 subcircuit, effectively raising and lowering it while the second LT1210 further amplifies the

Figure 2. Gain versus frequency plot of telescoping amplifier

input signal. This telescoping arrangement can be cascaded with additional stages to get more than ±30V. This amplifier is stable into capacitive loads, is short-circuit protected and thermally shuts down when overheated.

Extending Power Supply Voltages

Another method of getting high voltage from an amplifier is the extended-supply mode (see "Extending Op Amp Supplies to Get More Voltage"; *Linear Technology* Volume IV Number 2 (June 1994), pp. 20–22). This involves steering two external regulators with the power supply pins of an op amp to get a high voltage amplifier.

Figure 3 shows the LT1210 connected in the extended-supply mode. Placing an amplifier in the extended-supply mode requires changing the return of the compensation node from the power supply pins to system ground. R9 and C5 are selected for clean step response. The process of relocating the return of the compensation node slows the amplifier down to approximately 1MHz (see Figure 4). Figure 3's circuit will provide ±1A at ±100V, is stable into capacitive loads and is short-circuit protected. The two external MOSFETs need heat sinking.

Figure 1. Telescoping amplifiers

Figure 3. ±100V, ±1A power driver

$$A_V = -\frac{R8\,(R9 + R10)}{R8\,R9 - R7\,R10}$$

Gateway to the Stars

The circuit of Figure 3 can be expanded to yield much higher voltages; the first and most obvious way is to use higher voltage MOSFETs. This causes two problems: first, high voltage P-channel MOSFETs are hard to get; second, and more importantly, at ±1A the power dissipated by the MOS-FETs is too high for single packages. The solution is to build telescoping regulators, as shown in Figure 5. This circuit can provide ±1A of current at ±200V and has the additional power-dissipation ability of four MOSFETs.

Boosting Output Current

The current booster detailed in Figure 6 illustrates a technique for amplifying the output current capability of an op amp while maintaining speed. Among the many niceties of this topology is the fact that both Q1 and Q2 are normally off and thus consume no quiescent current. Once the load current reaches approximately 100mA, Q1 or Q2 turns on, providing additional drive to the output. This transition is seamless to the outside world and takes advantage of the full speed of Q1 and Q2. This circuit's small-signal bandwidth and full-power bandwidth are shown in Figure 7.
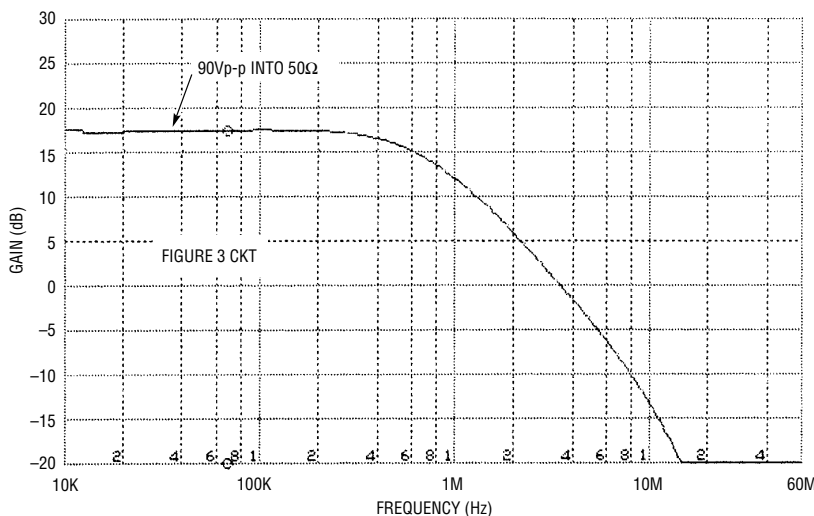
Boosting Both Current and Voltage

The current-boosted amplifier shown in Figure 6 can be used to replace the amplifiers in Figure 1, yielding ±10A at ±30V. Placing the boosted amplifier in the circuits shown in Figures 3 or 5 will yield peak powers into the kilowatts.

Thermal Management

When the LT1210 is used with external transistors to increase its output voltage and/or current range an additional benefit can often be realized: system thermal shutdown. Careful analysis of the thermal design of the system can coordinate the overtemperature shutdown of the LT1210 with the junction temperatures of the external transistors. This essentially extends the umbrella of protection of the LT1210's thermal

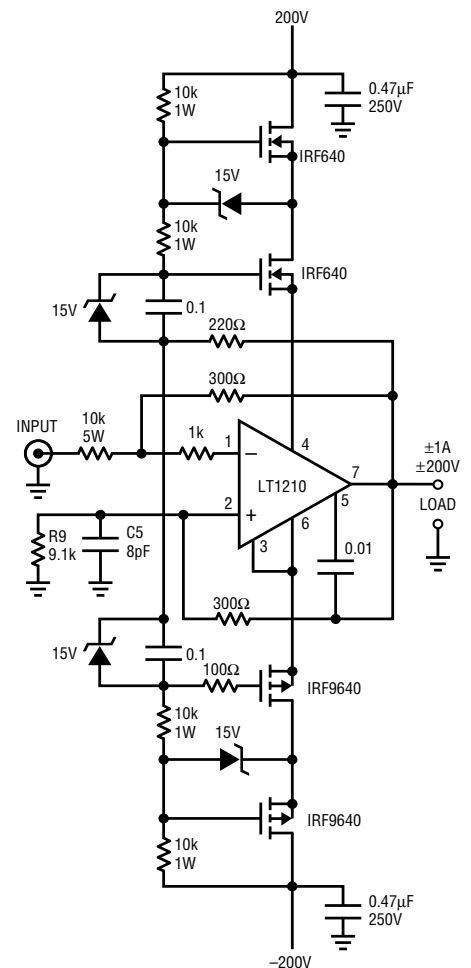**Figure 4. Gain versus frequency plot of extended-supply amplifier**

Figure 5. Cascode power amplifier

LTC1441-Based Micropower Voltage-to-Frequency Converter

by Jim Williams

Figure 1 is a voltage-to-frequency converter. A 0V–5V input produces a 0–10kHz output, with a linearity of 0.02%. Gain drift is 60ppm/°C. Maximum current consumption is only 26µA, 100 times lower than currently available units.

To understand the circuit's operation, assume that C1's negative input is slightly below its positive input (C2's output is low). The input voltage causes a positive-going ramp at C1's input (trace A, Figure 2). C1's output is high, allowing current flow from Q1's emitter, through C1's output stage to the 100pF capacitor. The 2.2µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 100pF unit charges is a function of Q1's emitter potential and Q6's drop. C1's CMOS output, purely ohmic, contributes no voltage error. When the ramp at C1's negative input goes high enough, C1's output goes low (trace B) and the inverter switches high (trace C). This action pulls current from C1's negative input capacitor via the Q5 route (trace D). This current removal resets C1's negative input ramp to a potential slightly below ground. The 50pF capacitor furnishes AC positive feedback (C1's positive input is trace E) ensuring that C1's output remains negative long enough for a complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The three LT1004s are the actual voltage reference and the LM334 current source provides 12µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by using the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2–Q4 trio. This correction's sign and magnitude directly oppose the –120ppm/°C 100pF polystyrene capacitor's drift,
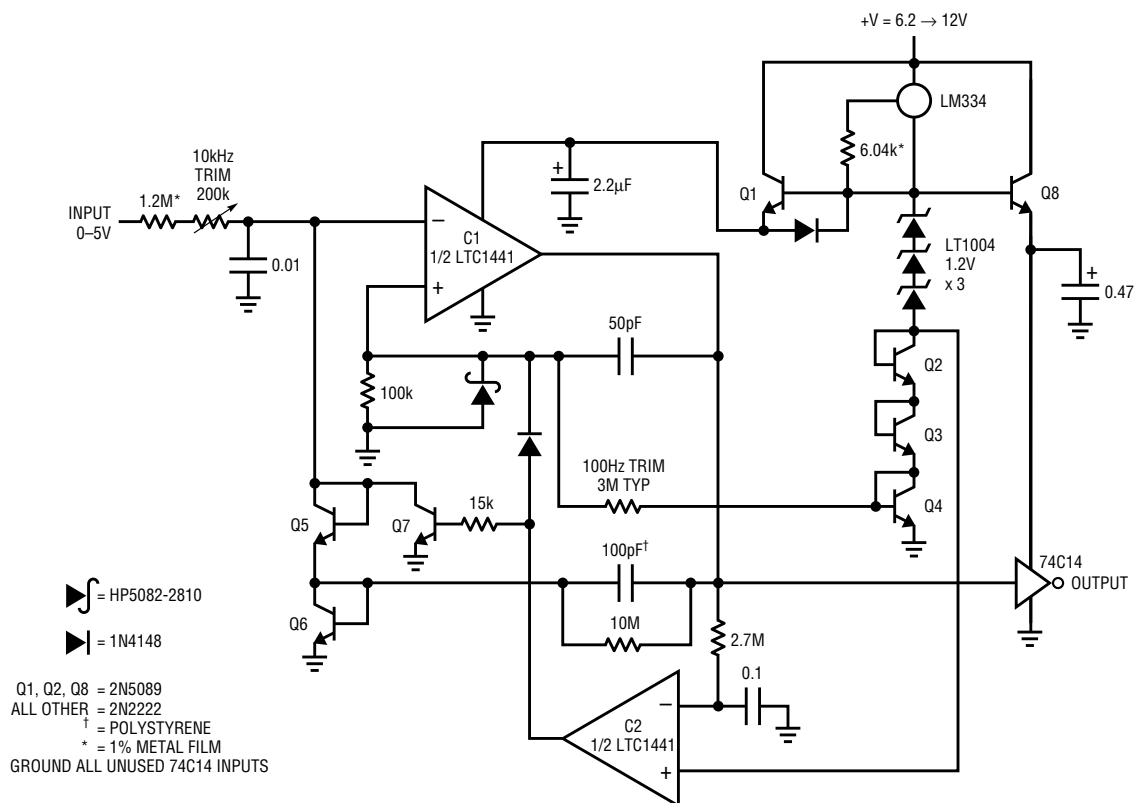

Figure 1. 0.02% V/F converter requires only 26µA supply current

aiding overall circuit stability. Q8's isolated 100pF drive to the CMOS inverter prevents output loading from influencing Q1's operating point. This makes circuit accuracy independent of loading.
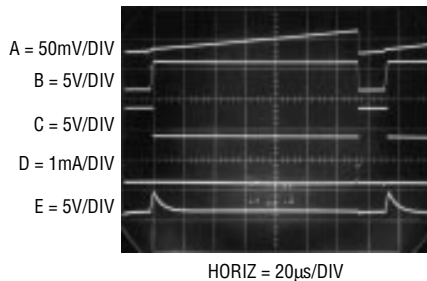
The Q1 emitter-follower delivers charge to the 100pF capacitor efficiently. Both base and collector current end up in the capacitor. The 100pF capacitor, as small as accu-

Figure 2. Waveforms for the micropower V/F converter: charge-based feedback provides precision operation with extremely low power consumption.

racy permits, draws only small transient currents during its charge and discharge cycles. The 50pF–100k positive feedback combination draws insignificantly small switching currents. Figure 3, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, comparator quiescent current and the 12µA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the 100pF capacitor's charge-discharge cycle introduces the 1.1µA/kHz increase shown. A smaller value capacitor would cut power, but effects of stray capacitance and charge imbalance would introduce accuracy errors.
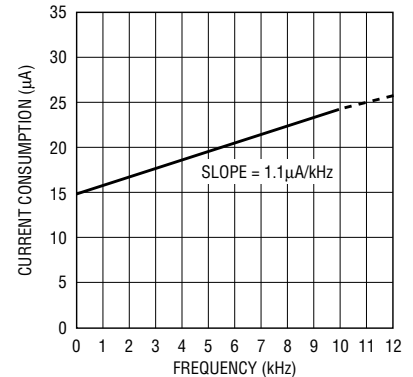
Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M–0.1µF lag, goes high. This lifts C1's positive input and

grounds the negative input with Q7, initiating normal circuit action.

To calibrate this circuit, apply 50mV and select the indicated resistor at C1's positive input for a 100Hz output. Complete the calibration by applying 5V and trimming the input potentiometer for a 10kHz output. ☇

Figure 3. Current consumption versus frequency for the V/F converter: charge/discharge cycles account for 1.1µA/kHz current drain increase.

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shutdown to cover the external transistors. The thermal shutdown of the LT1210 activates when the junction temperature reaches 150°C and has about 10°C hysteresis. The thermal resistance $R_{\theta JC}$ of the TO-220 package (LT1210CY) is 5°C/Watt).

Summary

The LT1210 is a great part; its performance in terms of speed, output current and output voltage is unsurpassed. Its C-Load™ output drive and thermal shutdown allow it to take its place in the real world—no kid gloves are required here. If the generous output specification of the

LT1210 isn't big enough for your needs, just add a couple of transistors to dissipate the additional power and you are on your way. Only the worldwide supply of transistors limits the amount of power you could command with one of these parts. ☇
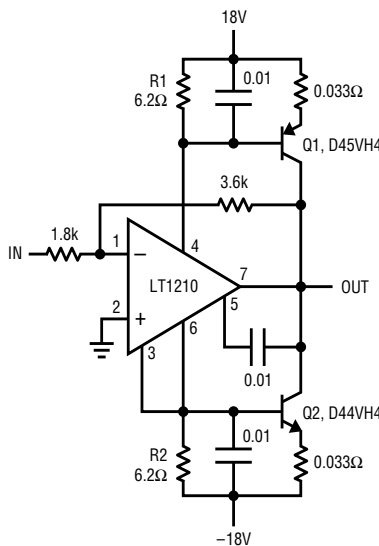
Figure 6. ±10A/1MHz current-boosted power op amp
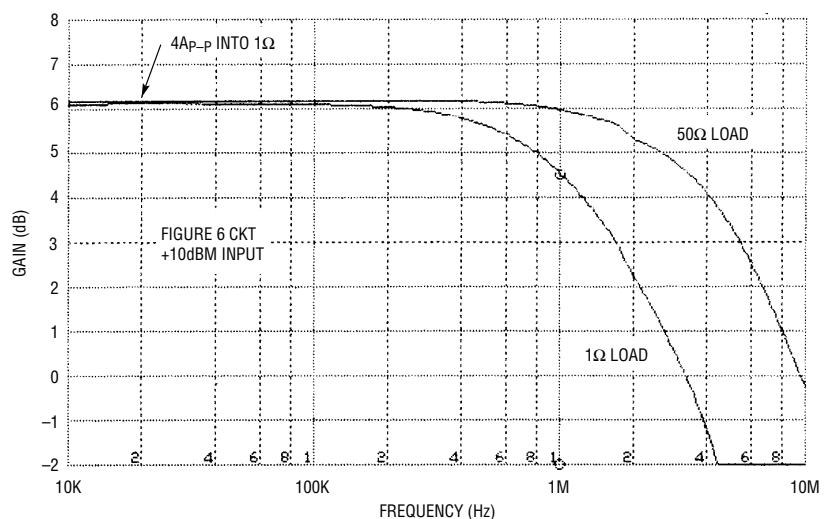
Figure 7. Gain versus frequency response of current-boosted amplifier

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Capacitive Charge Pump Powers 12V VPP from 5V Source

by Mitchell Lee

The LTC1263, a regulating charge pump tripler, converts a 5V input to a regulated 12V, 60mA output. No inductors are required; charge pumps operate with capacitors only. Figure 1 shows the LTC1263 configured to provide VPP for two flash memory chips. The "flying" capacitors in the charge pump, C1 and C2, are sized well within the surface mount ceramic range. C_{IN} and C_{OUT}, as shown, are surface mount tantalum capacitors, such as Sprague 595D series. In the 10µF capacitance range, tantalum capacitors cost less than ceramic units. The chip operates by charging C1 and C2 in parallel across 5V and ground and then discharging them in series across 5V and the output. In theory, the output could reach 15V, but an internal regulation loop maintains the output at a constant 12V.

SHUTDOWN reduces the quiescent current of the LTC1263 to less than 1µA under logic control. In shutdown mode, the output is held at 5V by an internal 500Ω, V_{CC}-to-V_{OUT} switch. Output-voltage fall time is guaranteed to be less than 15ms for the component values shown. Output rise time coming out of shutdown is guaranteed to be less than 800µs.

Designing a circuit to generate a split supply from a single 5V source is usually an unpleasant chore; one to be avoided at all costs. If load current requirements are modest, the LTC1263 can generate both 12V and –7V for op amps and biasing needs. Figure 2 shows how. The LTC1263 is connected in the usual way to produce a regulated, 12V output, but a 2 diode, 2-capacitor charge pump is added to the C2+ pin. This pin switches between V_{CC} and V_{OUT}, swinging approximately $7V_{P-P}$. The result is an outboard charge pump inverter with a –7V output.

Schemes like this one often suffer from poor cross regulation. Although the inverting output is not directly regulated, the –7V load does affect the 12V output, thereby improving cross regulation (see Figure 3). The regulation with a common load (such as op amps) is shown in Figure 4. *LT*
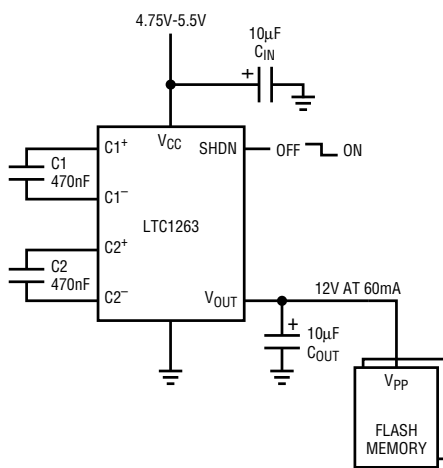

Figure 1. Programming two flash chips with the LTC1263 charge pump. In shutdown mode, the output is held at 5V.
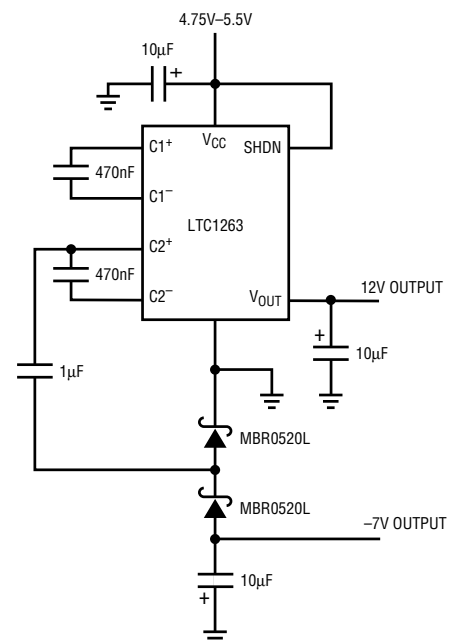
Figure 2. Split supply generator: cross regulation is improved by driving the inverting charge pump from C2+.

Figure 3. Cross regulation with a constant 12V load

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

Figure 4. Output regulation with a common load

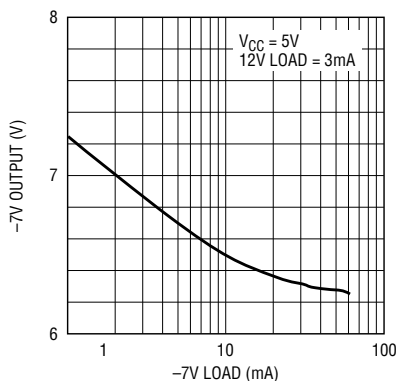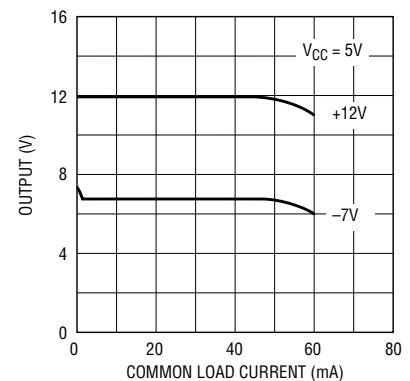# Bridge Measures Small Capacitance in Presence of Large Strays
by Jeff Witt

Capacitance sensors measure a wide variety of physical quantities, such as position, acceleration, pressure and fluid level. The capacitance changes are often much smaller than stray capacitances, especially if the sensor is remotely placed. I needed to make measurements with a 50pF cryogenic fluid level detector, with only 2pF full-scale change, hooked to several hundred pF of varying cable capacitance. This required a circuit with high stability, sensitivity and noise rejection, but one insensitive to stray capacitance caused by cables and shielding. I also wanted battery operation and analog output for easy interfacing to other instruments. Two traditional circuit types have drawbacks: integrators are sensitive to noise at the comparator and voltage-to-frequency converters typically measure stray as well as sensor capacitance. The capacitance bridge presented here measures small transducer capacitance changes, yet rejects noise and cable capacitance.

The bridge, shown in Figure 1, is designed around the LTC1043 switched-capacitor building block. The circuit compares a capacitor, C_X, of unknown value, with a reference capacitor, C_{REF}. The LTC1043, programmed with C1 to switch at 500Hz, applies a square wave of amplitude V_{REF} to node A, and a square wave of amplitude V_{OUT} and opposite phase to node B. When the bridge is balanced, the AC voltage at node C is zero, and

$$V_{OUT} = V_{REF} \frac{C_X}{C_{REF}}$$

Balance is achieved by integrating the current from node C using an op amp (LT1413) and a third switch on the LTC1043 for synchronous detection. With $C_{REF} = 500pF$ and $V_{REF} = 2.5V$, this circuit has a gain of 5mV/pF, and when measured with a DMM achieves a resolution of 10fF for a dynamic range of 100dB. It also rejects stray capacitance (shown as ghosts in Figure 1) by 100dB. If this rejection is not important, the switching frequency f can be increased to extend the circuit's bandwidth, which is

$$BW = f \frac{C_{REF}}{C_{OUT}}$$

C_{OUT} should be larger than C_{REF}.

The circuit operates from a single 5V supply and consumes 800μA. If the capacitances at nodes A and C are kept below 500pF, the LT1078 micropower dual op amp may be used in place of the LT1413, reducing supply current to just 160μA.

If the relative capacitance change is small, the circuit can be modified for higher resolution, as shown in Figure 2. A JFET input op amp (LT1462) amplifies the signal before demodulation for good noise performance, and the output of the integrator is attenuated by R1 and R2 to increase the sensitivity of the circuit. If $\Delta C_X \ll C_X$, and $C_{REF} \approx C_X$, then

$$V_{OUT} - V_{REF} \approx V_{REF} \frac{\Delta C_X (R1 + R2)}{C_{REF} R2}$$

With $C_{REF} = 50pF$, the circuit has a gain of 5V/pF and can resolve 2fF. Supply current is 1mA. The synchronous detection makes this circuit insensitive to external noise sources and in this respect shielding is not terribly important. However, to achieve high resolution and stability, care should be taken to shield the capacitors being measured. I used this circuit for the fluid level detector mentioned above, putting a small trim cap in parallel with C_{REF} to adjust offset and trimming R2 for proper gain.
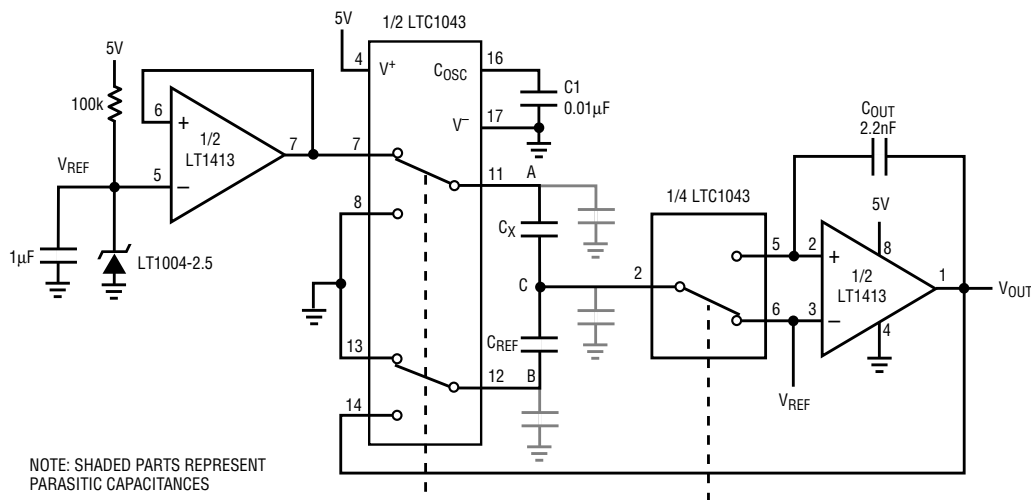

NOTE: SHADED PARTS REPRESENT PARASITIC CAPACITANCES

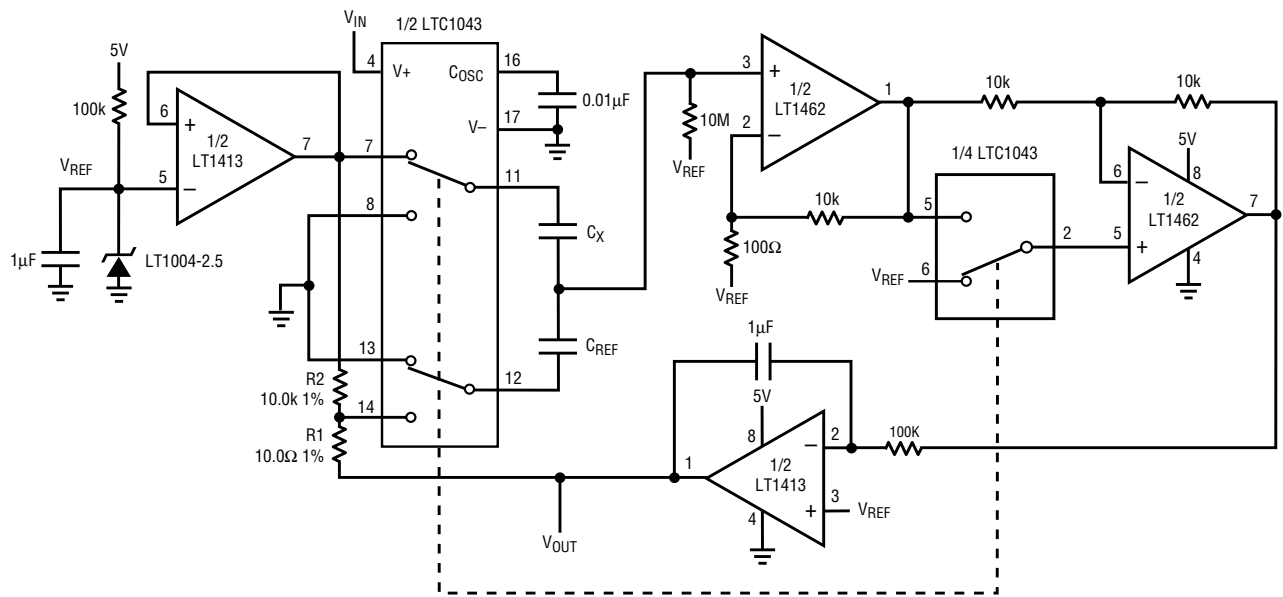**Figure 1. A simple, high performance capacitance bridge**

Figure 2. A bridge with increased sensitivity and noise performance

Bridge circuits are particularly suitable for differential measurements. When C_X and C_{REF} are replaced with two sensing capacitors, these circuits measure differential capacitance changes, but reject common mode changes. CMRR for the circuit in Figure 2 exceeds 70dB. In this case, however, the output is linear only for small relative capacitance changes. *LT*

LTC1433/44, continued from page 14

the internal sense resistance. Figures 6 and 7 show the dropout characteristic at different load currents.

Power-On Reset Monitor Included

An internal regulation monitor provided in the LTC1433 and LTC1434 continuously monitors the output. When the device is out of regulation or in shutdown mode, the POR open drain output pulls low. At start-up, once the output voltage has reached 5% of its final value, an internal timer is started, after which the POR pin is released. The timer counts 2^{16} oscillator cycles, yielding a delay-to-release reset of approximately 300ms in a typical application. Once the output is in regulation, it has to fall by 7.5% before the POR pin is asserted.
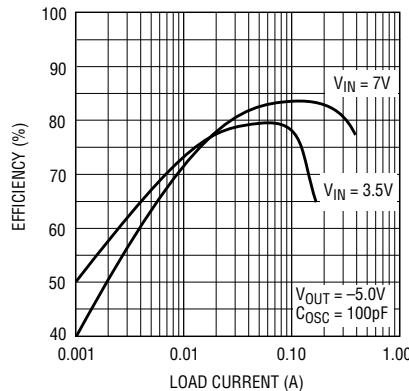

Figure 9. Efficiency curve for Figure 8's positive-to-negative converter

Typical Application: Positive-to-Negative Converter

Both the LTC1433 and LTC1434 can easily be set up for a negative output voltage. Figure 8 shows the schematic using the LTC1433. The

efficiency curve is shown in Figure 9. This circuit is set up so that the output is taken from the device ground. Components that are referenced back to the device ground, Run/SS capacitor, oscillator frequency capacitor and I_{TH} compensation network, are connected to the output instead of to the circuit ground.

Conclusion

The LTC1433 and LTC1434, with their low dropout, high efficiency and small footprint, are ideal for battery-operated portable equipment applications. In addition, their constant frequency operation makes the devices suited for applications that require the switching regulator to operate at a defined frequency. *LT*

DESIGN TOOLS

Applications on Disk

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp.

Available at no charge.

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim.

Available at no charge.

SwitcherCAD — SwitcherCAD is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD — MicropowerSCAD is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices.

$10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992.

The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge

Power Solutions Brochure — This 80 page collection of circuits contains real-life solutions for common power supply design problems. There are over 79 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators and switched capacitor conversion. Available at no charge.

High Speed Amplifier Solutions Brochure — This 72 page collection of circuits contains real-life solutions for problems that require high speed amplifiers. There are 82 circuits including descriptions, graphs and performance specifications. Topics covered include basic amplifiers, video-related applications circuits, instrumentation, DAC and photodiode amplifiers, filters, variable gain, oscillators and current sources and other unusual application circuits. Available at no charge

Data Conversion Solutions Brochure — This 52 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected Application and Design Notes is also included. Available at no charge

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